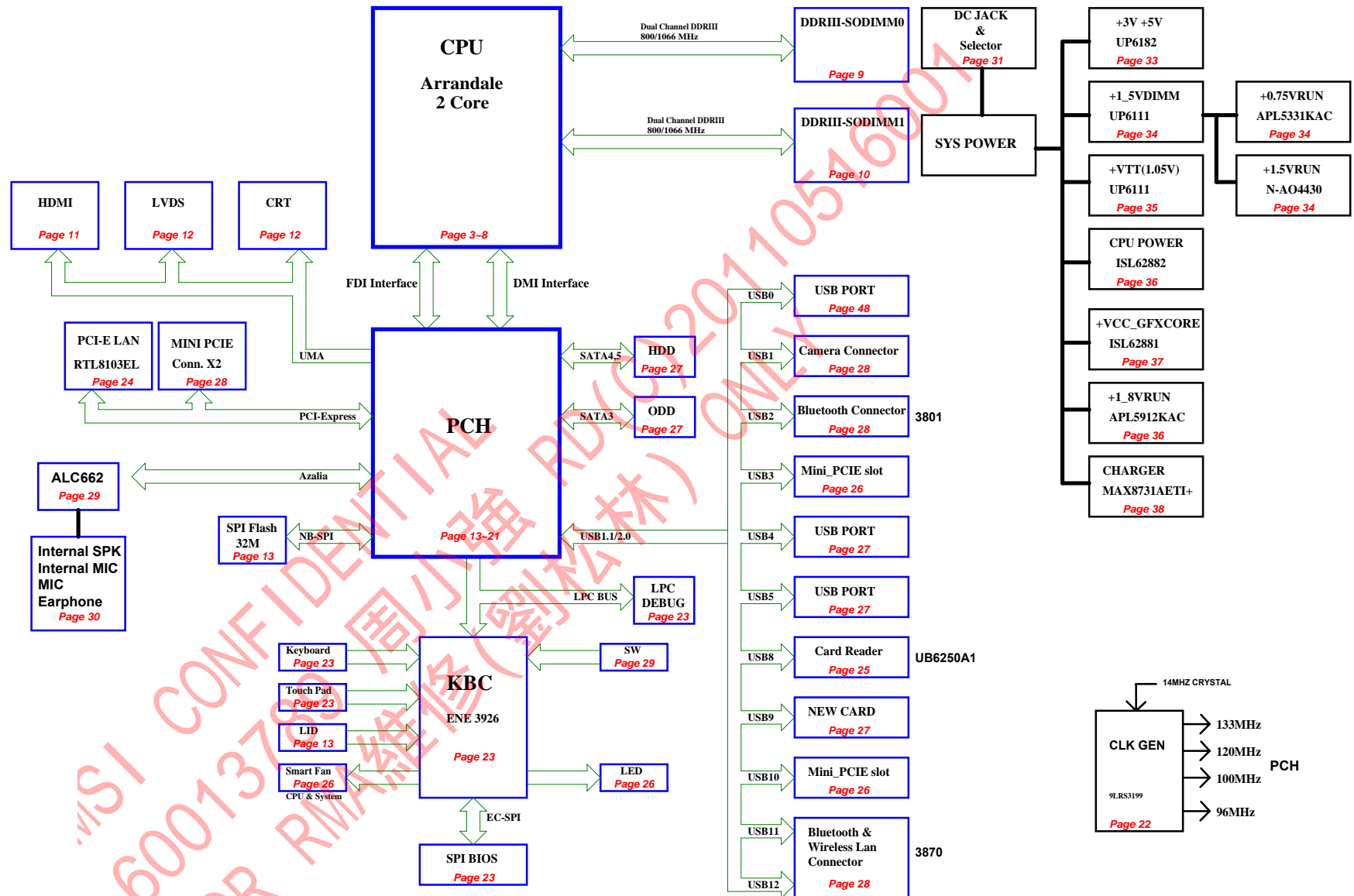


Calpella Platform

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SCHEMATIC ANNOTATIONS AND BOARD INFORMATION

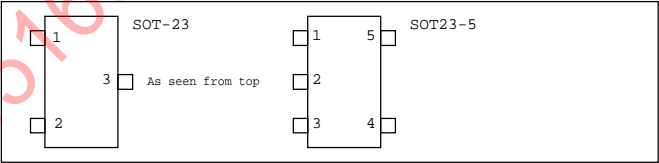
Voltage Rails

POWER PLANE	VOLTAGE	ACTIVE IN	DESCRIPTION
PWR_SRC	19V	S0,(S3-S5)	LAN
+5VALW	5V	S0,(S3-S5)	
+5VRUN	5V	S0	
+5VSUS	5V	S0	
+3VALW	3.3V	S0,(S3-S5)	
+3VSUS	3.3V	S0,(S3-S5)	DDRIII core
+3VRUN	3.3V	S0	
+1_5VDIMM	1.5V	S0,S3	
+1_5VRUN	1.5V	S0	PCH DDRIII command & control pull up. CPU core rail Graphics core rail (Dual Core only)
VTT	1.05V	S0	
+0_75VRUN	0.75V	S0	
+VCC_CORE	1.05V~1.1V	S0	
+VCC_GFXCORE	1.1V	S0	

Net Naming Conventions

Suffix
= Active Low Signal
Prefix
H = Host
M = DDR Memory
TP = Test Point (does not connect anywhere else)

PCB Footprints



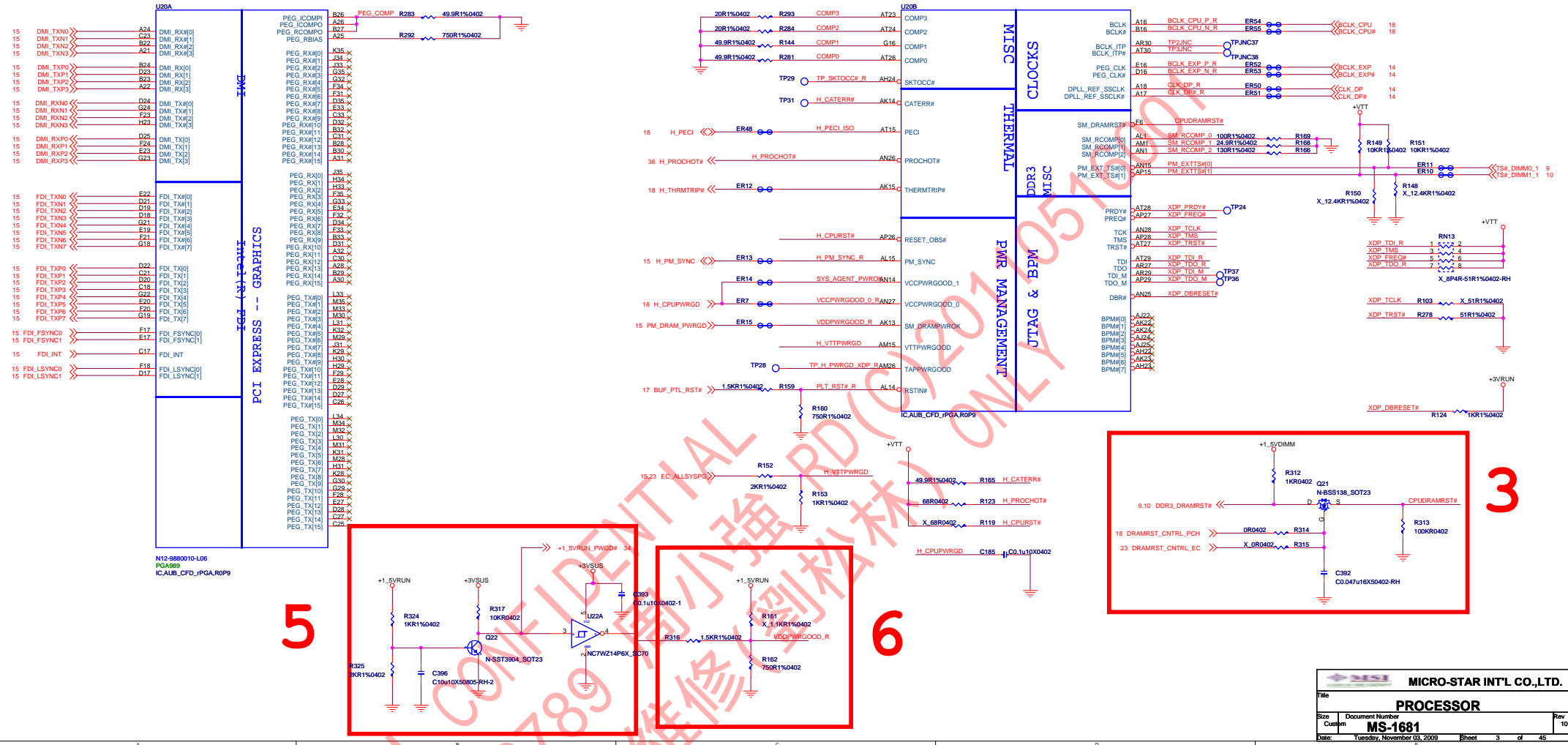
AC Mode

Power States	SLP_S3#	SLP_S4#	SLP_S5#	SLP_LAN#	+V*ALWAYS	+V*SUS	+V*RUN	CLK
S0 (Full on)	HIGH	HIGH	HIGH	HIGH	ON	ON	ON	ON
S3 (Suspend to RAM)	LOW	HIGH	HIGH	HIGH	ON	ON	OFF	OFF
S4 (Suspend to Disk)	LOW	LOW	HIGH	HIGH	ON	ON	OFF	OFF
S5 (Soft Off)	LOW	LOW	LOW	HIGH	ON	ON	OFF	OFF

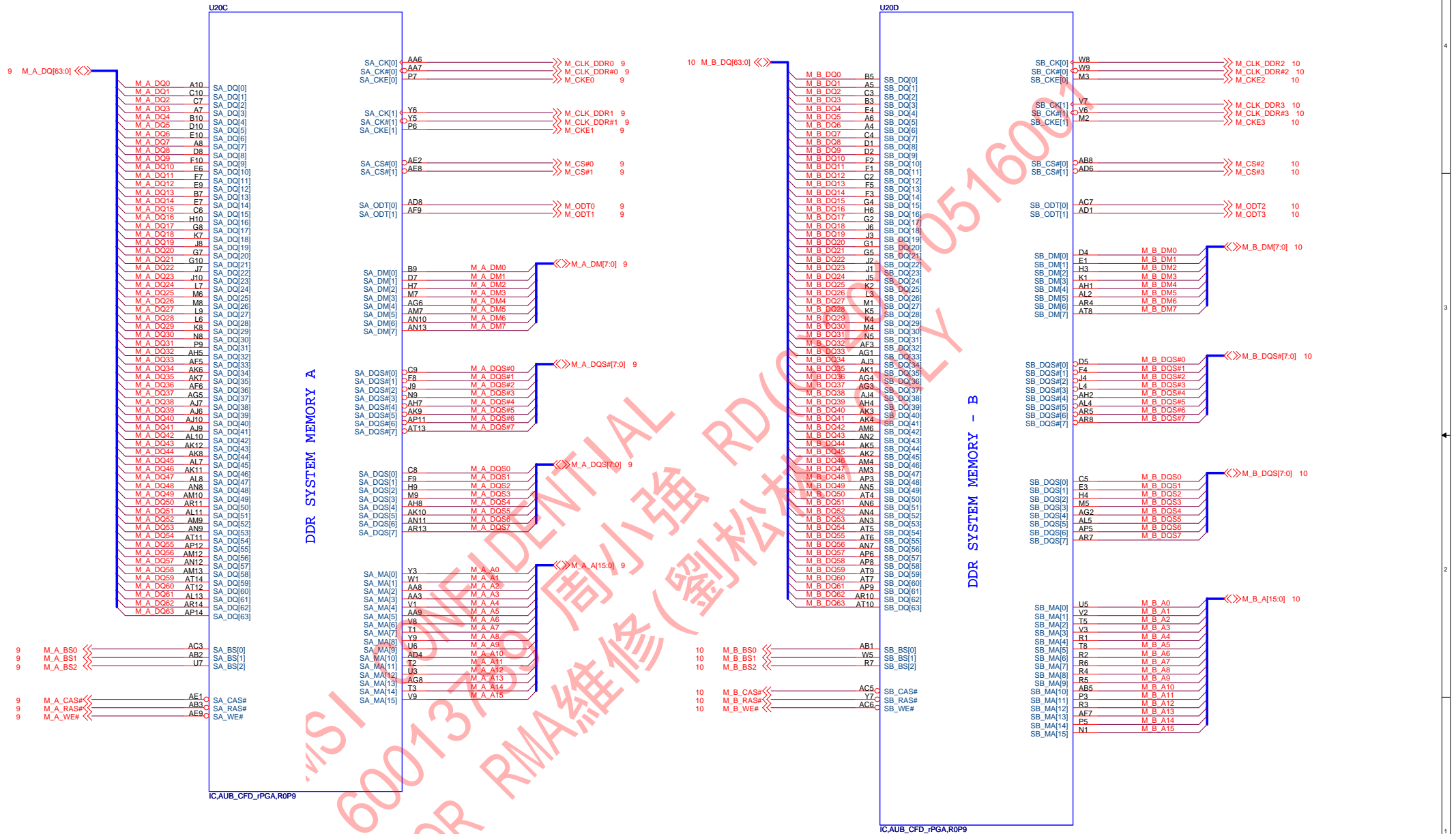
Battery Mode

Power States	SLP_S3#	SLP_S4#	SLP_S5#	SLP_LAN#	+V*ALWAYS	+V*SUS	+V*RUN	CLK
S0 (Full on)	HIGH	HIGH	HIGH	HIGH	ON	ON	ON	ON
S3 (Suspend to RAM)	LOW	HIGH	HIGH	HIGH	ON	ON	OFF	OFF
S4 (Suspend to Disk)	LOW	LOW	HIGH	HIGH	ON	OFF	OFF	OFF
S5 (Soft Off)	LOW	LOW	LOW	HIGH	ON	OFF	OFF	OFF

ARRANDALE PROCESSOR (CLK,MISC,JTAG)



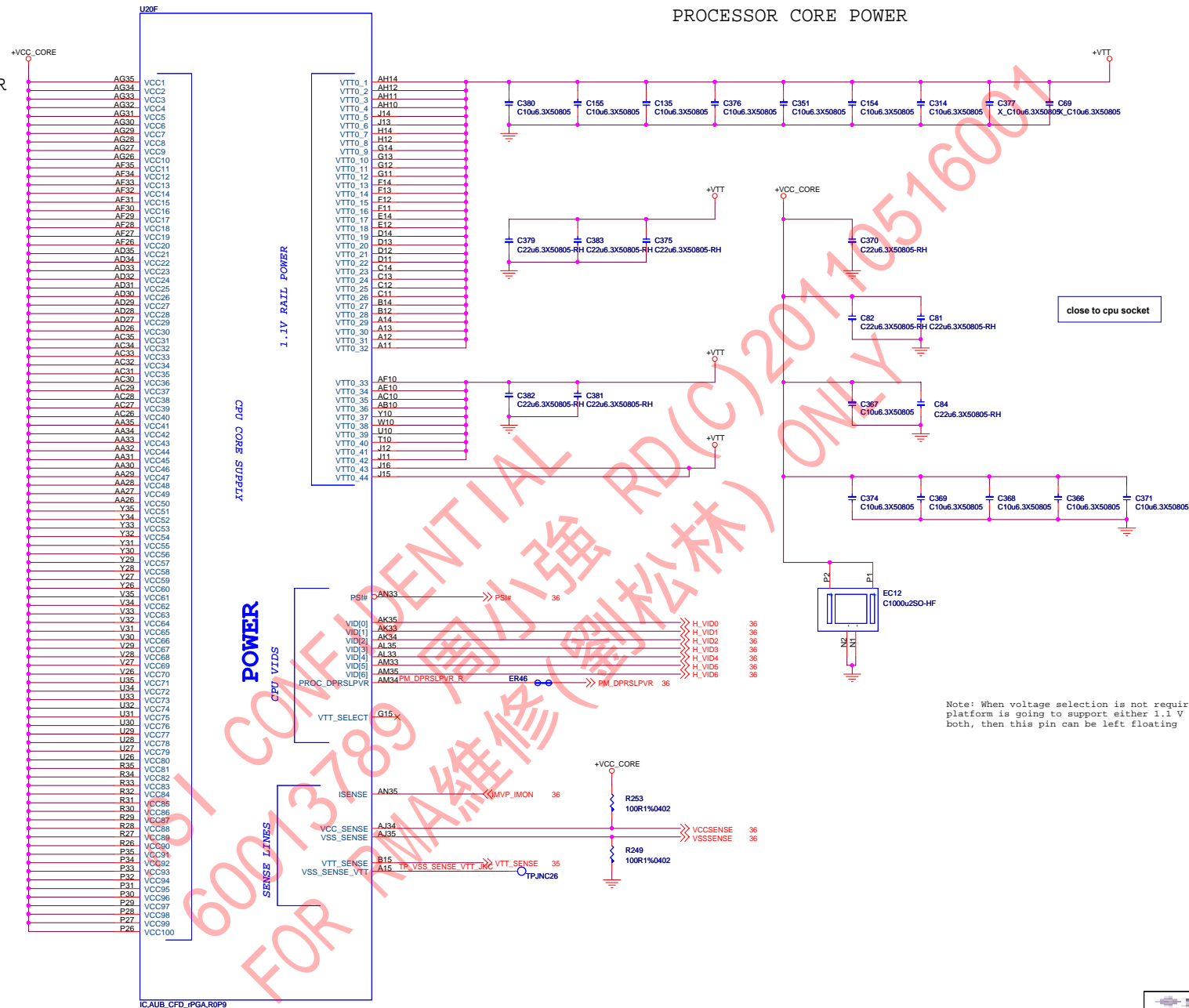
ARRANDALE PROCESSOR (DDR3)



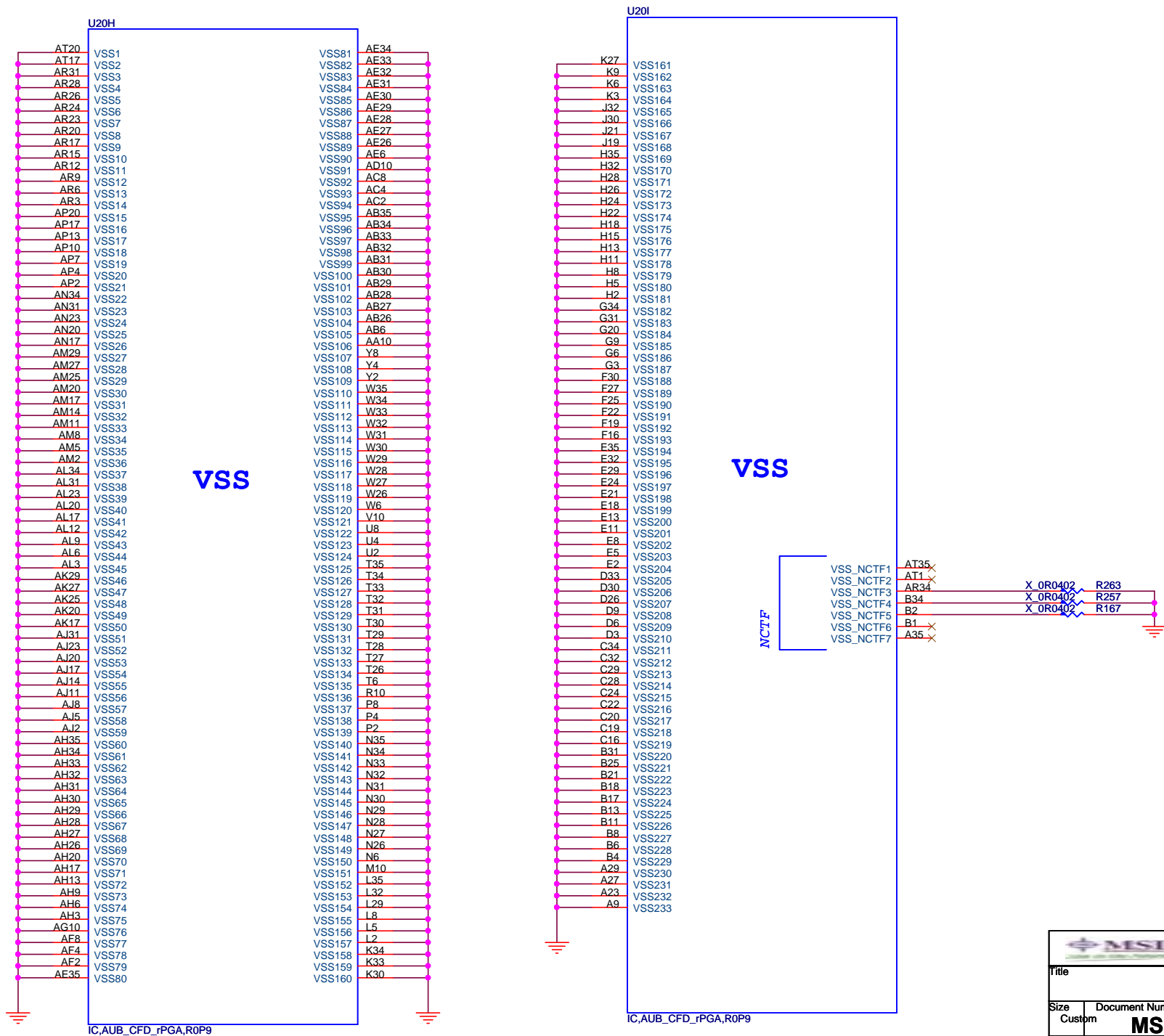
ARRANDALE PROCESSOR (POWER)

PROCESSOR CORE POWER

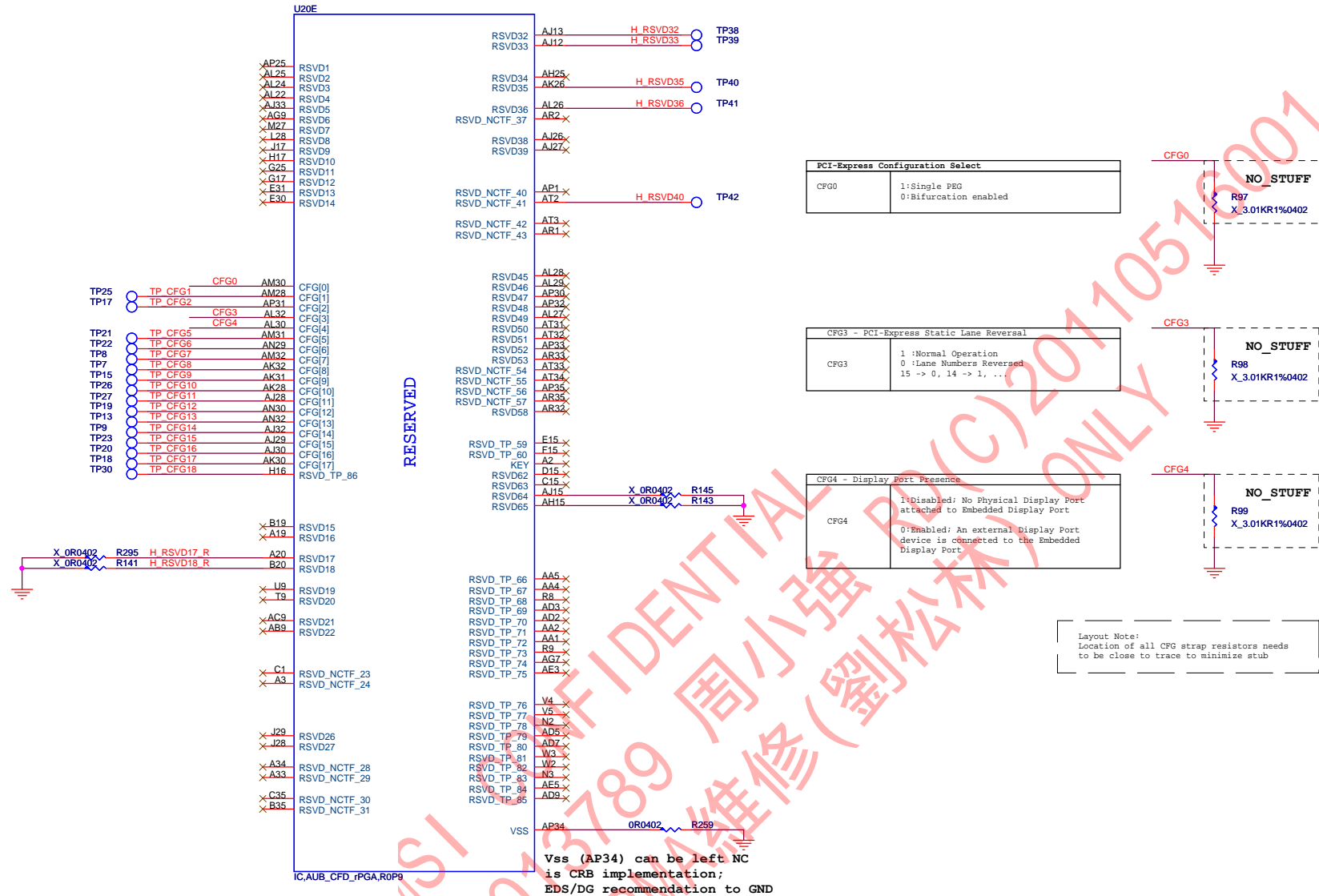
PROCESSOR CORE POWER



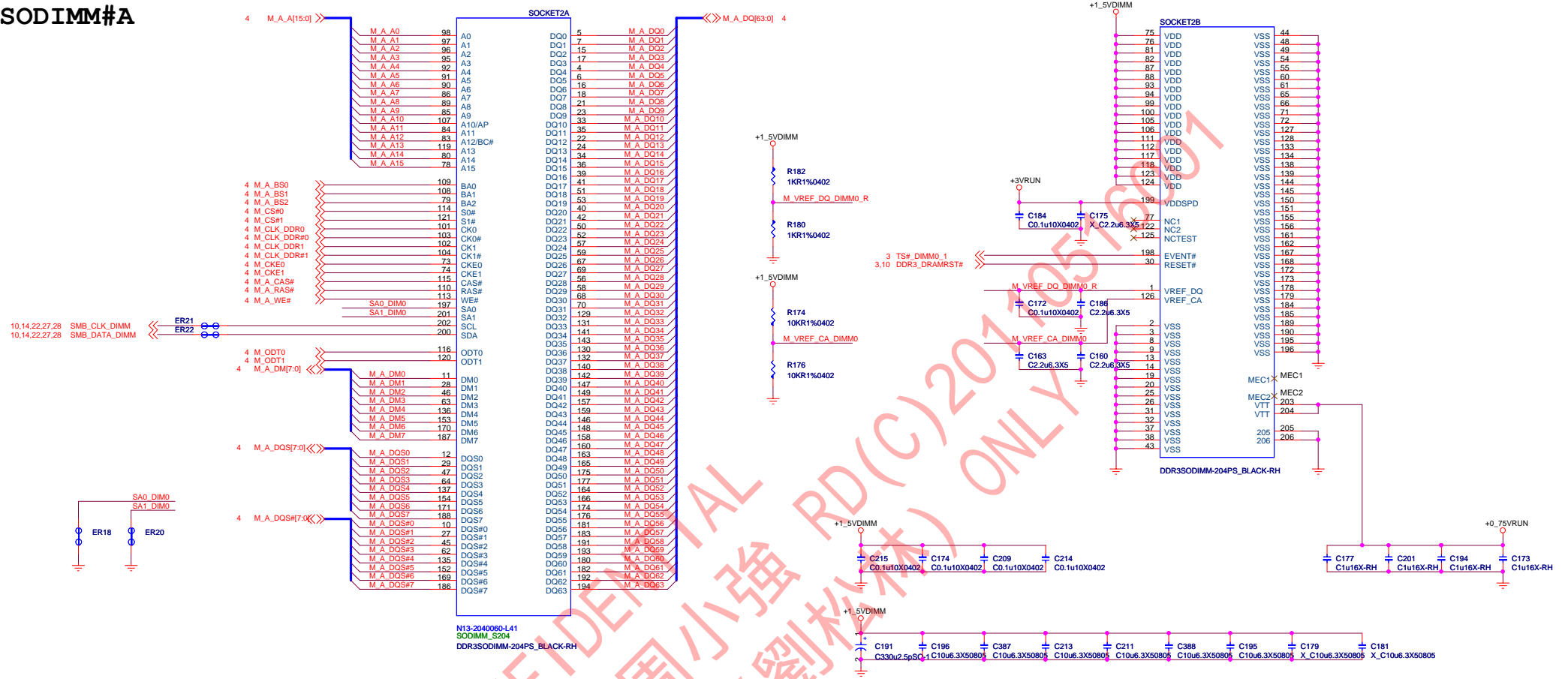
ARRANDALE PROCESSOR (GND)



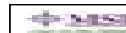
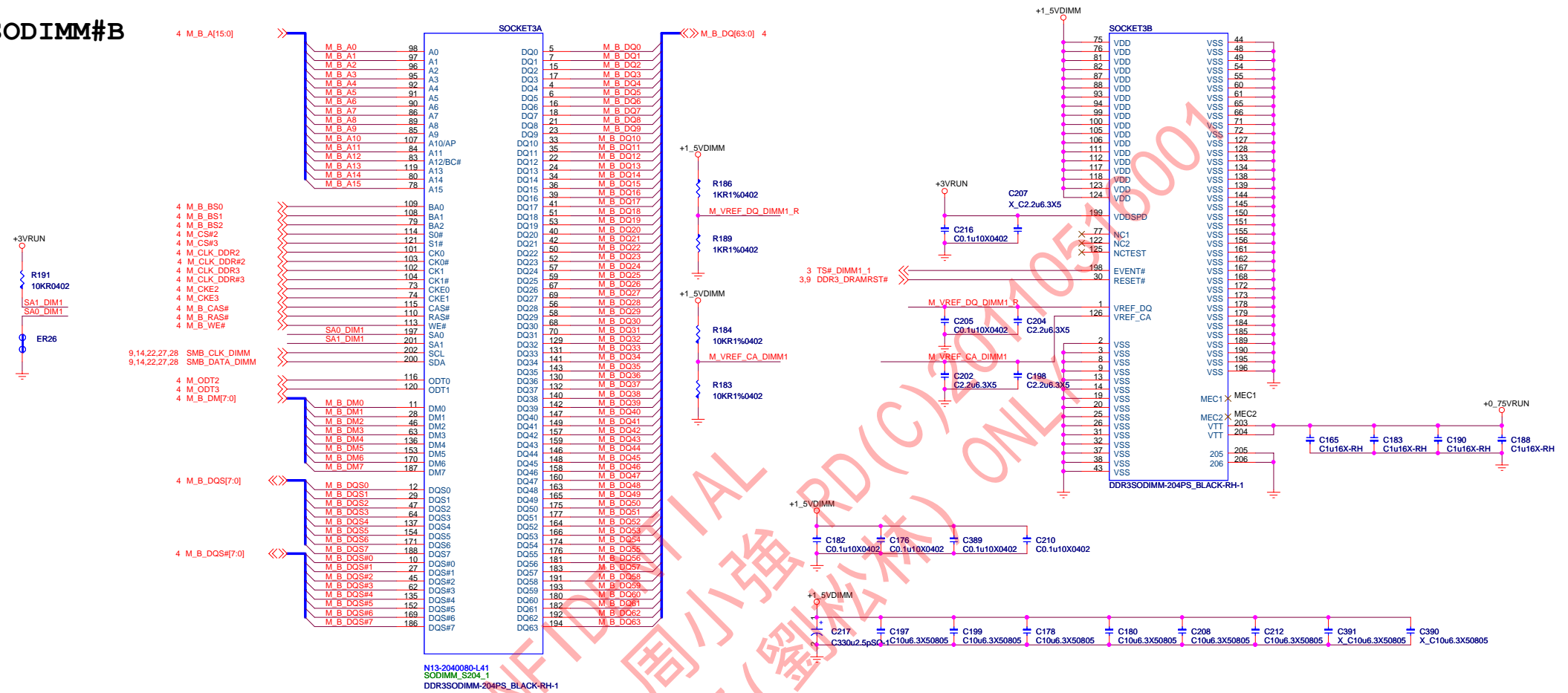
ARRANDALE PROCESSOR (RESERVED)



SODIMM#A



SODIMM#B



MICRO-STAR INT'L CO.,LTD.

[illegible]

DDR3 SODIMM1

Size

Document Number

Customer	
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MS-1681

Date: _____

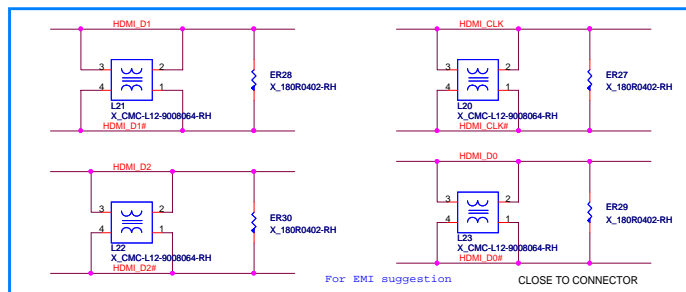
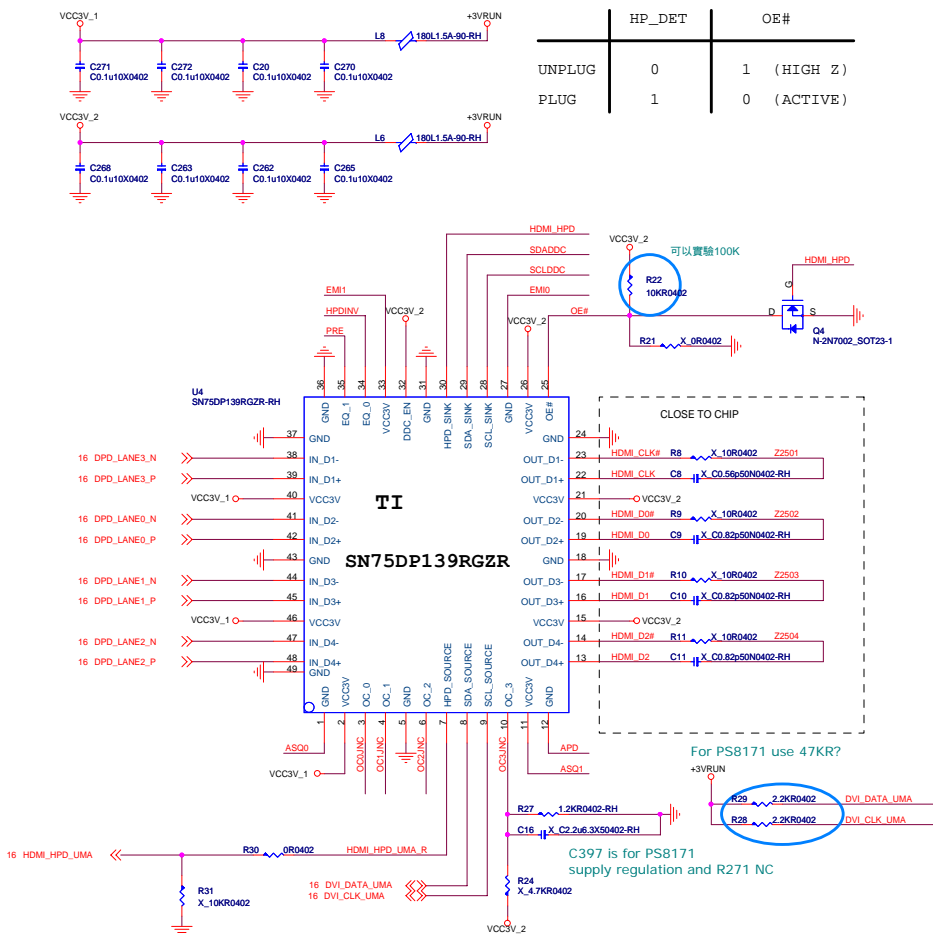
MC-1001
Tuesday, November 03

Sheet

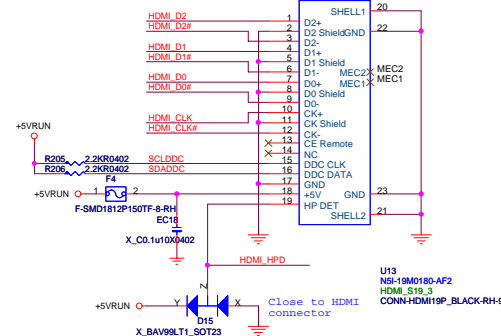
10

	Rev 10
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HDMI Switch

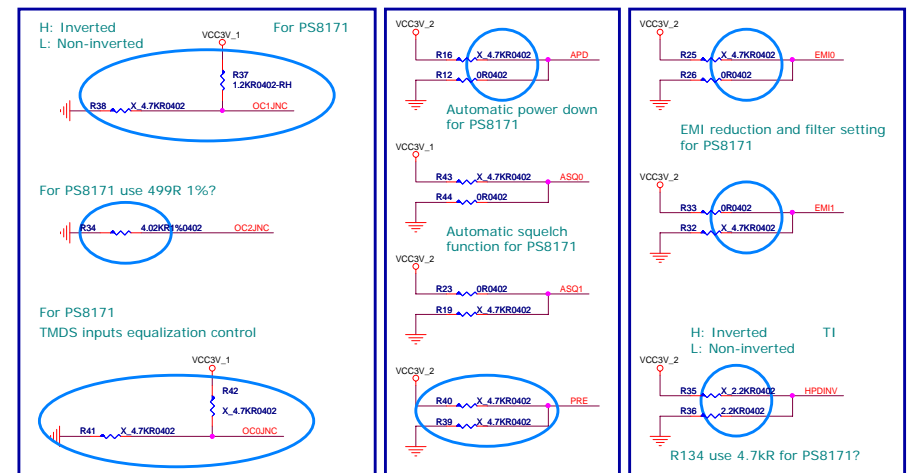


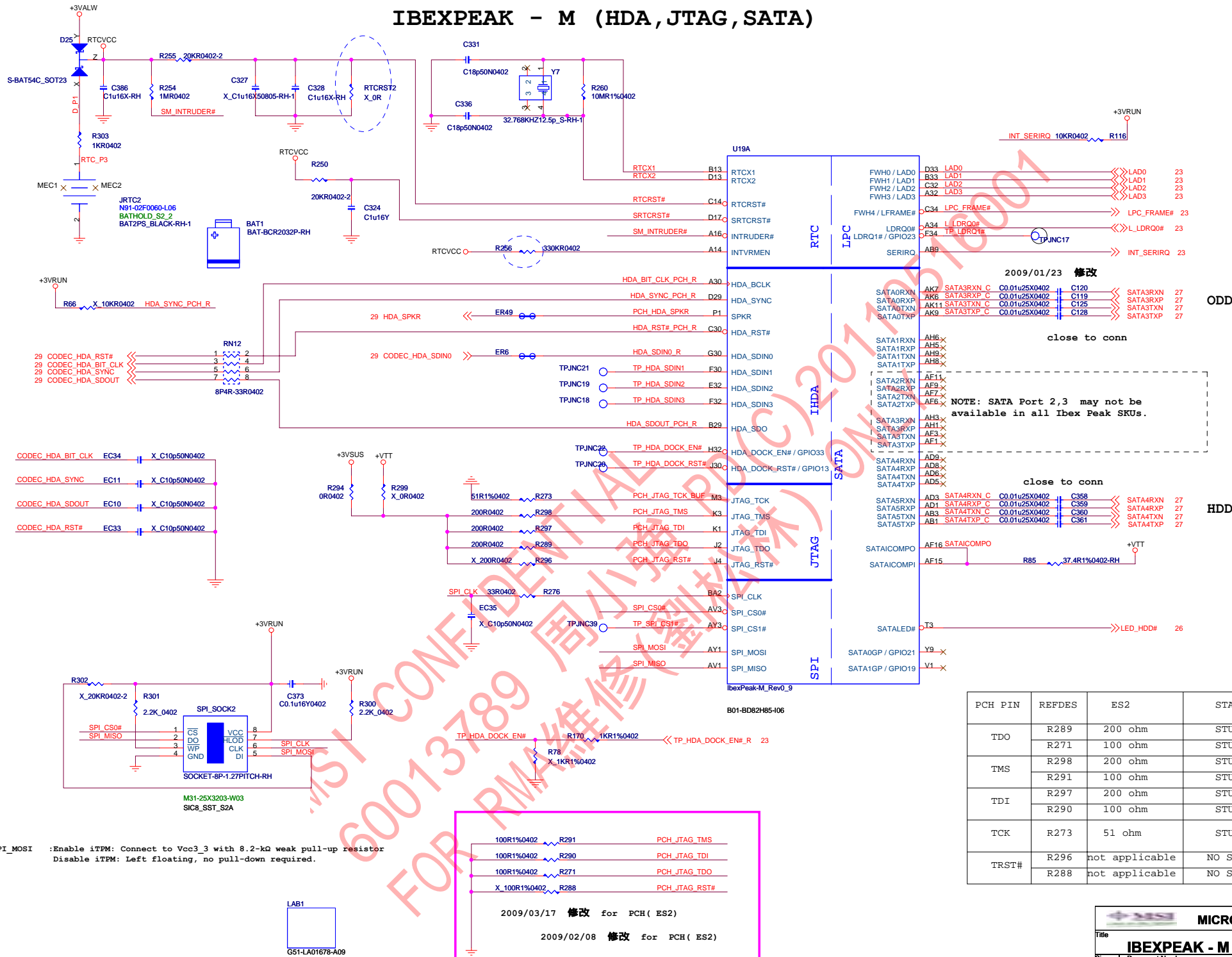
HDMI connector



SN75TDP139	PS8171		Pin no.
Floating	TMDS inputs equalization control (internal pull-down~500KΩ) PEQ = LOW: Mid level EQ (Default) PEQ = HIGH: High level EQ PEQ = MID: Low level EQ		Pin 3
High	(Internal pull down~500KΩ) PIO = LOW: HPD = HPD_SINK @ 3.3V CMOS output PIO = High: HPD= HPD_SINK# (inverted HPD) @ 0.5V		Pin 4
GND	[ASQ1,ASQ0] = HL: No automatic squelch (internal pull down~500kΩ) LI: Automatic squelch enable, Level = 120mVpp, default timer LH: Automatic squelch enable, Level = 100mVpp, default timer HH: Automatic squelch enable, Level = 80mVpp, default timer ML: Automatic squelch enable, Level = 120mVpp, extended timer MH: Automatic squelch enable, Level = 100mVpp, extended timer LM: Automatic squelch enable, Level = 80mVpp, extended timer HM: Reserved MM: Reserved	Pin 1	
VCC		Pin 11	
4.65K to GND	499R to GND		Pin 6
GND	Automatic power down management (Internal pull up~500KΩ) APD = LOW: Automatic power down disable APD = HIGH: Automatic power down enable APD = MID: Reserved		Pin 12
1.2K to GND	2.2uF to GND		Pin 10
GND	EMI reduction and filter setting. (EMI1 internal pull up~500KΩ; EMI0 internal pull down~500KΩ) (EMI1,EMI0) = HL: No EMI reduction EM10 = HIGH: Reduced rise/fall time MID: Reduced rise/fall time, 2nd EMI1 = LOW: EMI filter setting 1 MID: Reserved	Pin 27	
VCC		Pin 33	
Note2	DDC Active Buffer enable and setting (internal pull-down~500KΩ) DDCBUF = LOW: No DDC active buffer, passive DDC level shifting DDCBUF = HIGH: Active DDC buffer enable, setting 1 DDCBUF = MID: Active DDC buffer enable, setting 2		Pin 34
Floating	TMDS output driver pre-emphasis level setting (internal pull down~500KΩ) PRE = LOW No pre-emphasis PRE = HIGH: Low level pre-emphasis is added PRE = MID: High level pre-emphasis is added		Pin 35

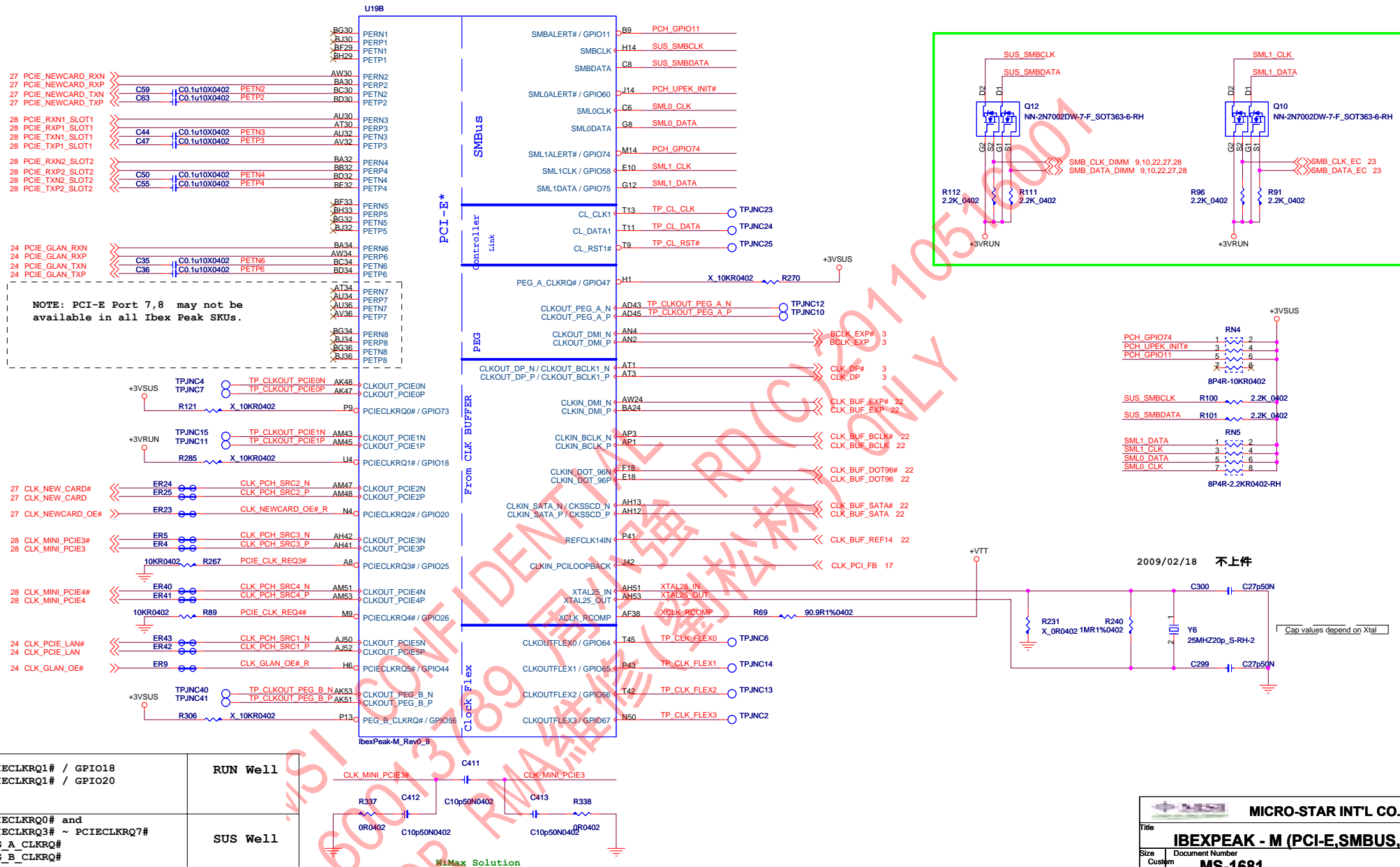
Note2: High is HPD logic inverted, Low is HPD logic non-inverted



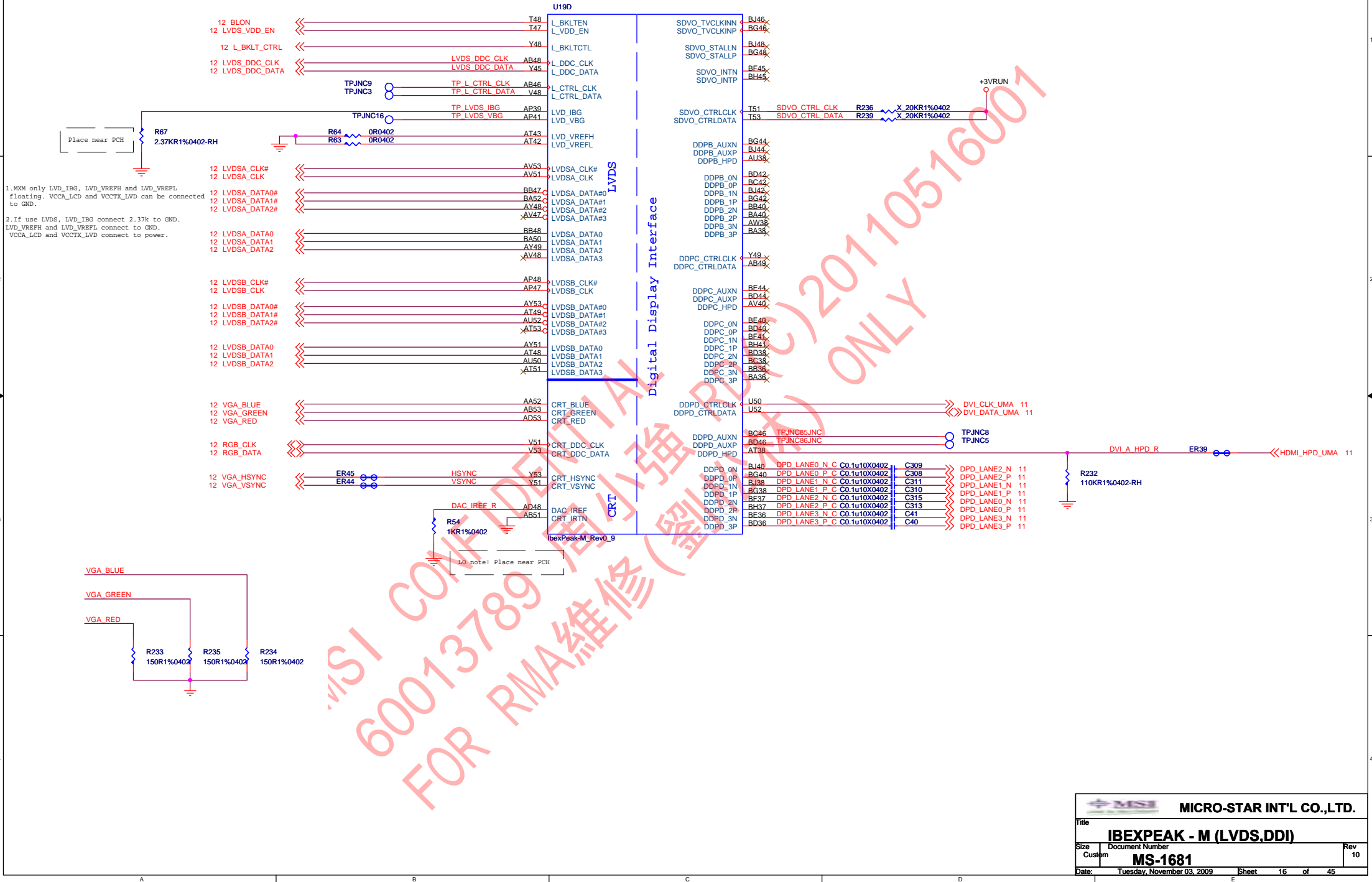
IBEXPEAK - M (HDA, JTAG, SATA)

PCH PIN	REFDES	ES2	STATE
TDO	R289	200 ohm	STUFF
	R271	100 ohm	STUFF
TMS	R298	200 ohm	STUFF
	R291	100 ohm	STUFF
TDI	R297	200 ohm	STUFF
	R290	100 ohm	STUFF
TCK	R273	51 ohm	STUFF
TRST#	R296	not applicable	NO STUFF
	R288	not applicable	NO STUFF

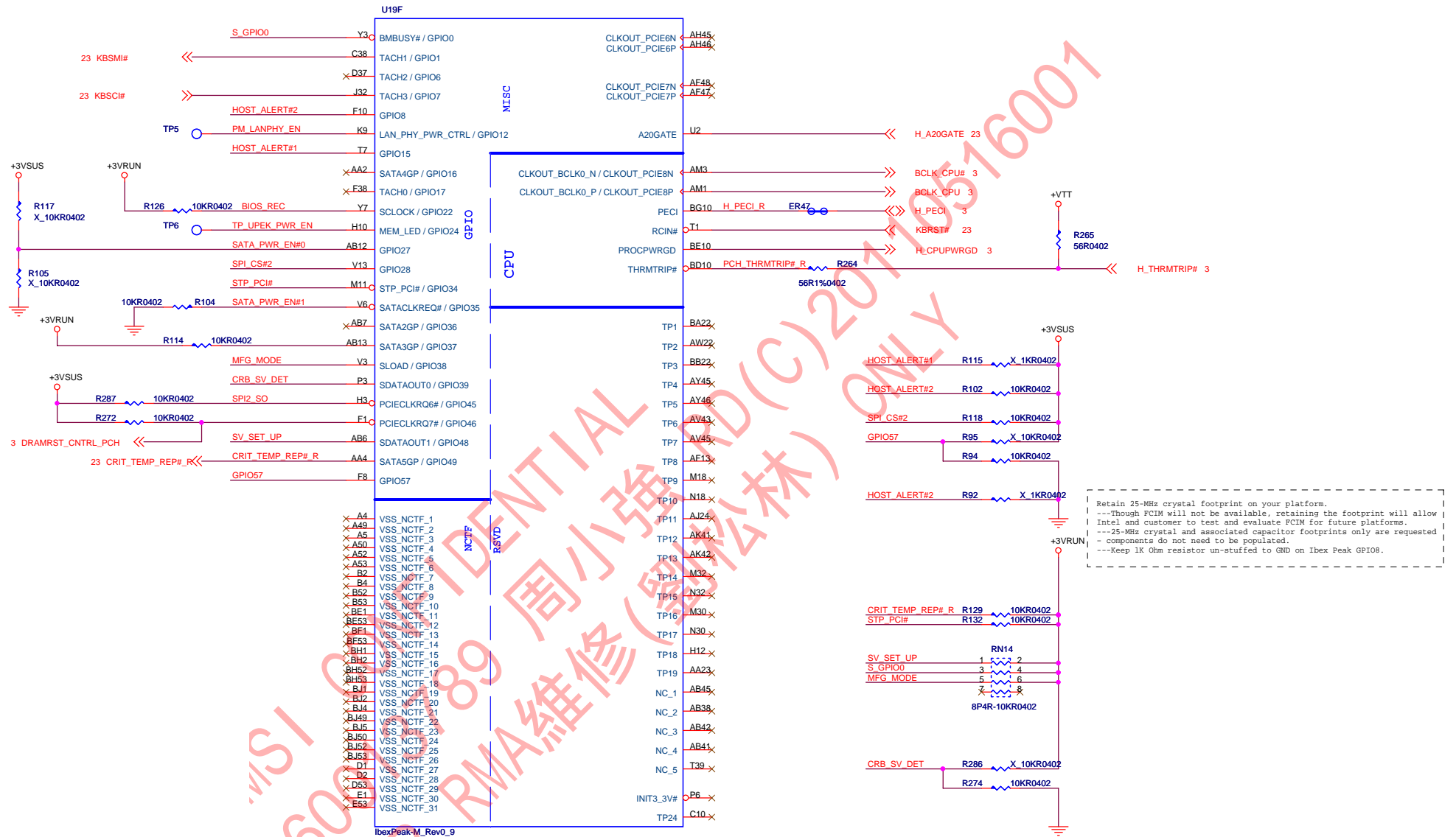
IBEXPEAK - M (PCI-E, SMBUS, CLK)



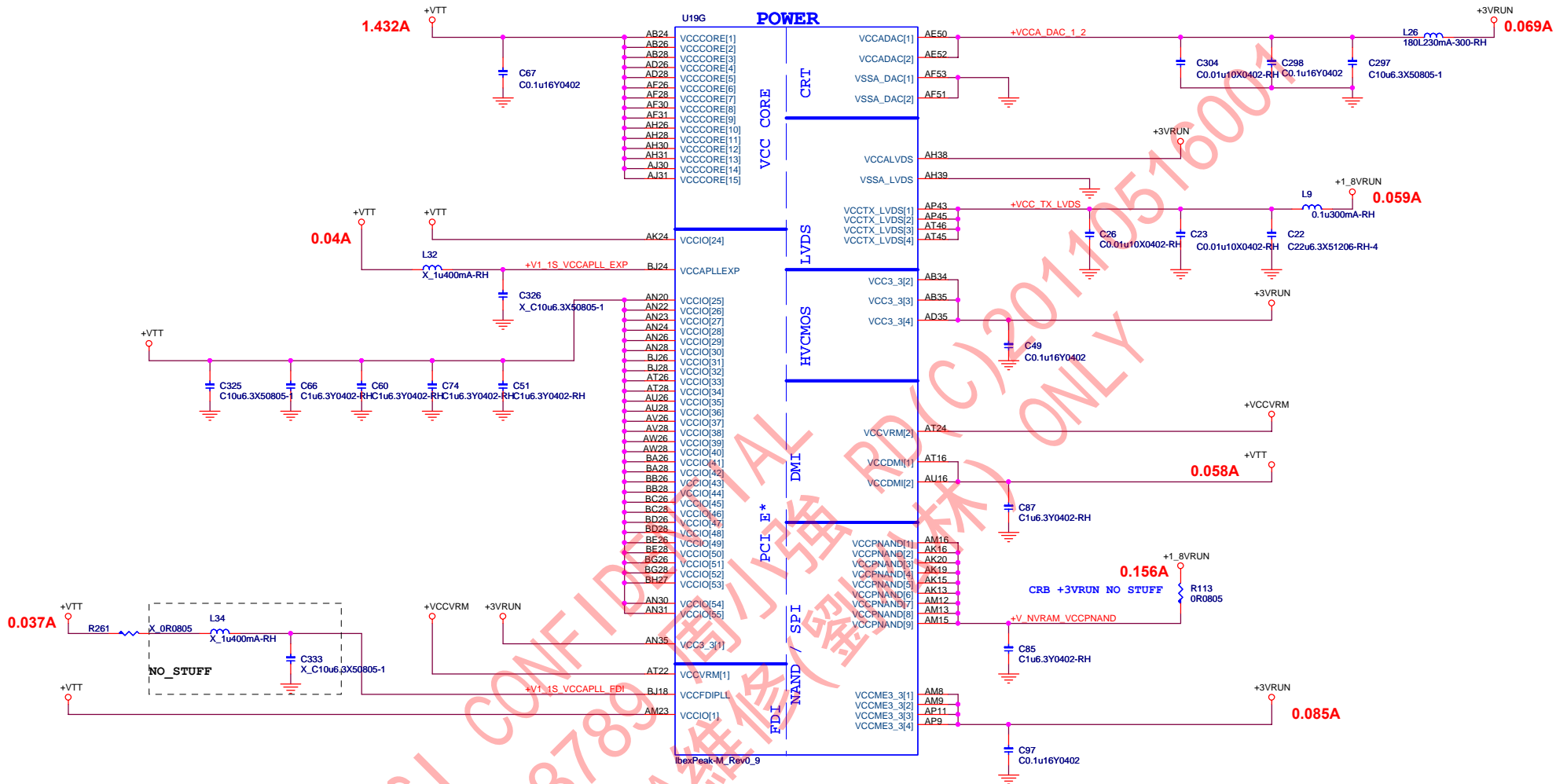
IBEXPEAK - M (LVDS,DDI)



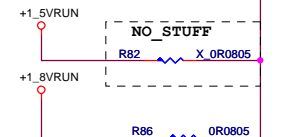
IBEXPEAK - M (GPIO,VSS_NCTF,RSVD)



IBEXPEAK - M (POWER)

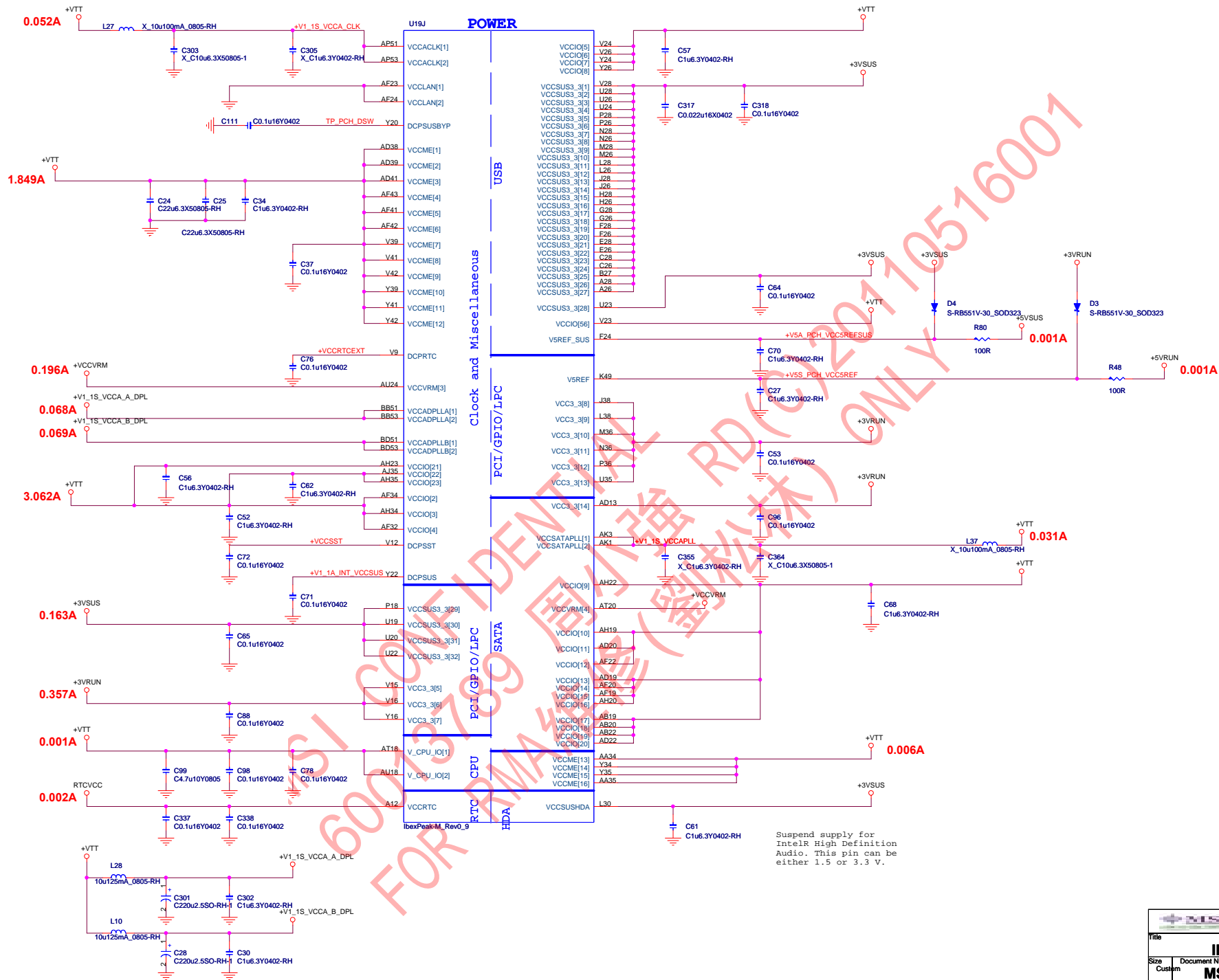


The VCCVCRM rail (1.8 V/1.5 V) powers an internal voltage regulator module (VRM) that regulates clean 1.05-V voltage supply for analog rails (VCCAClk, VccapllEXP, VCCFDIPLL, and VCCSATAPLL). This solution will allow us to remove the LC filter requirements for those rails, thereby reducing platform BOM cost. VCCVCRM is enabled by default via internal pull up to GPIO27, therefore GPIO27 should be left as No Connect. The following diagram shows implementation details on how to enable and disable VccVRM.



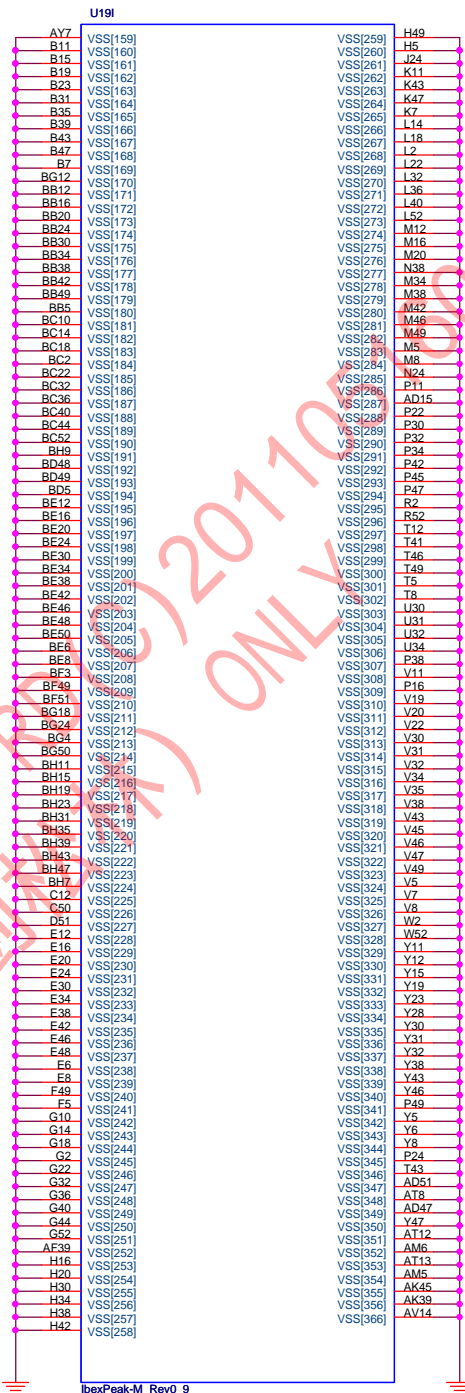
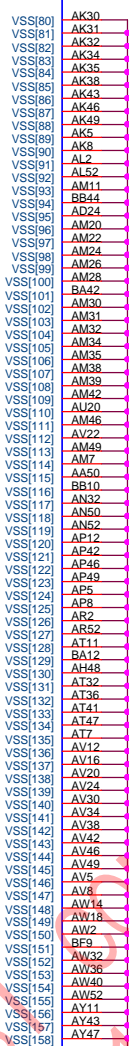
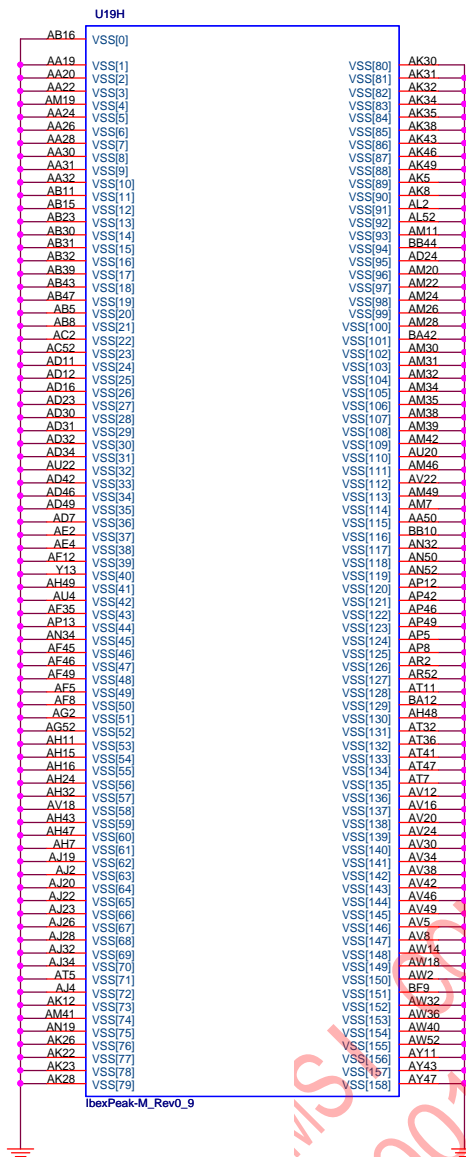
VccLAN may be grounded if Intel LAN is disabled.

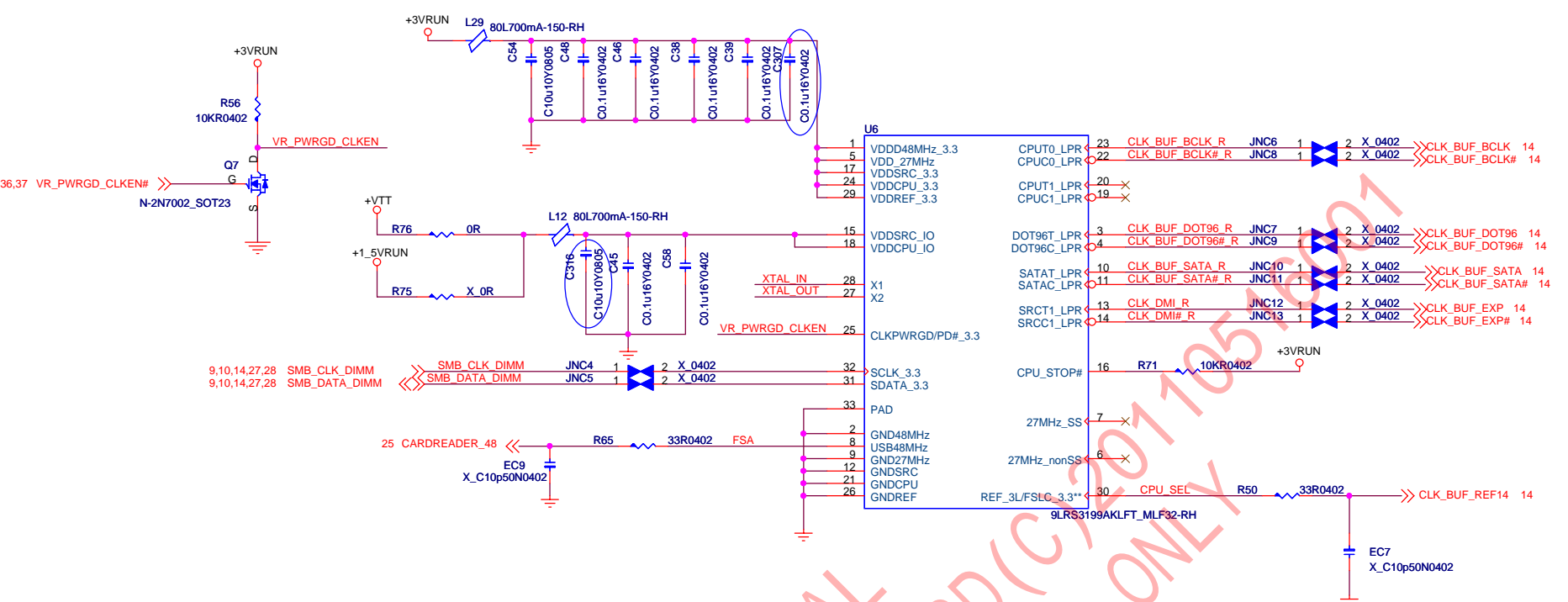
IBEXPEAK - M (POWER)



Suspend supply for Intel® High Definition Audio. This pin can be either 1.5 or 3.3 V.

IBEXPEAK - M (GND)





Capacity select
If LC=20pf C708/C709=33pf
If LC=32pf C708/C709=56pf



For CPU frequency select (133MHz)

CPU_SEL	CPU0	CPU1
0(Default)	133MHz	133MHz
1(1.05~1.5V)	100MHz	100MHz

Co-Lay Note:

For IDT IC9IRS3199
R598,R599,R600=10Kohm

For Sillego SLG8SP587
R598,R599,R600=4.7Kohm

Date:

Tuesday, November 03, 2009

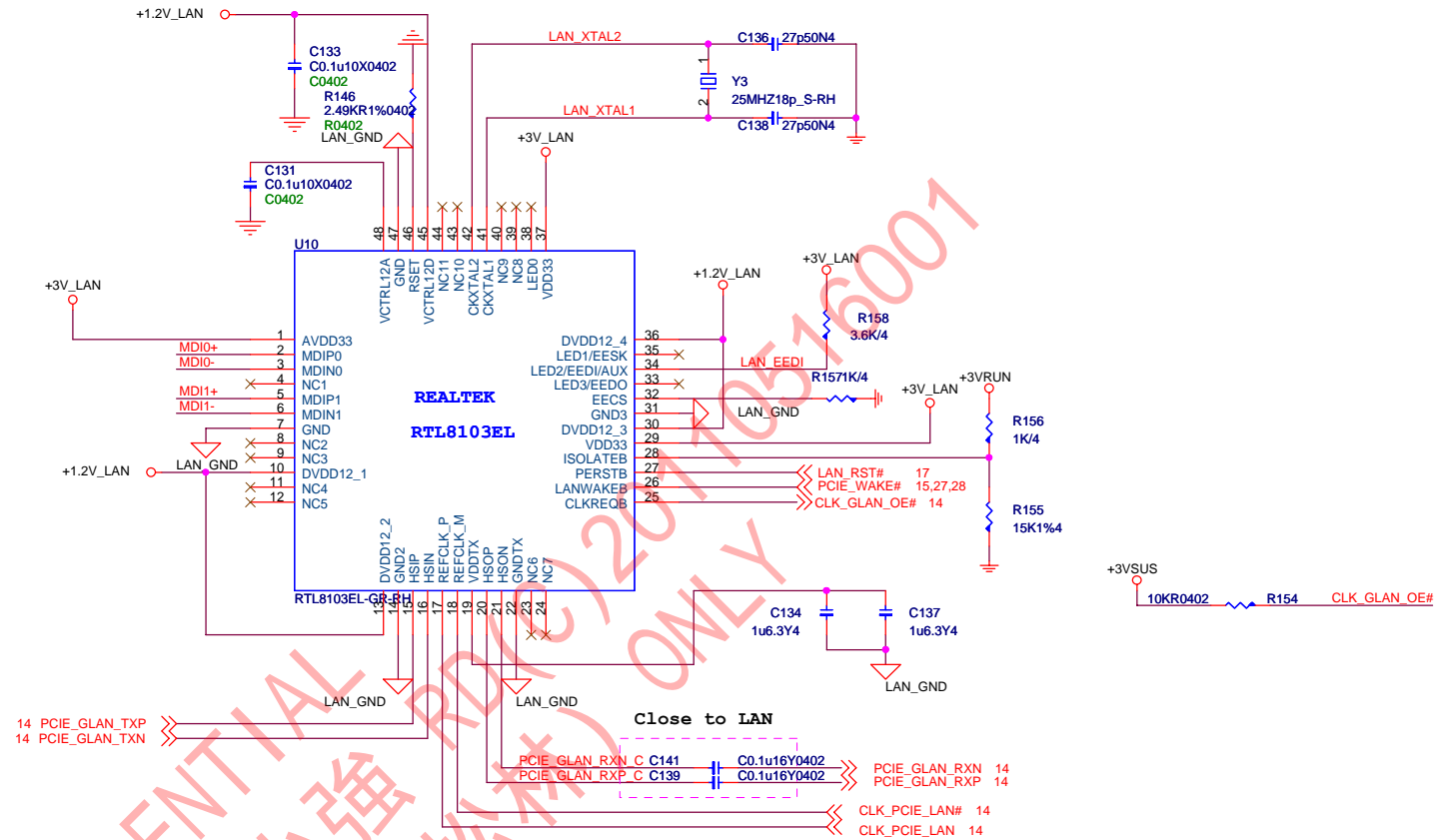
Sheet

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of

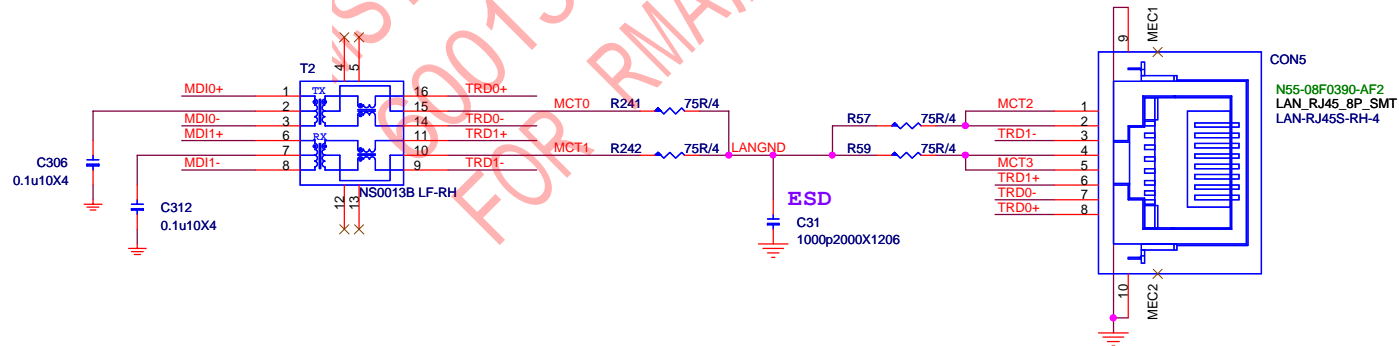
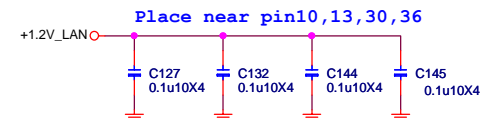
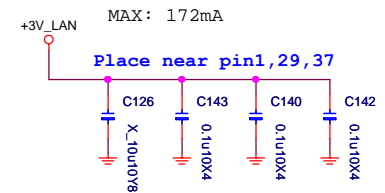
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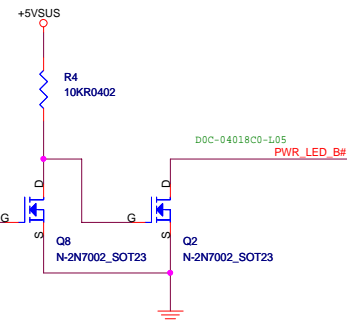
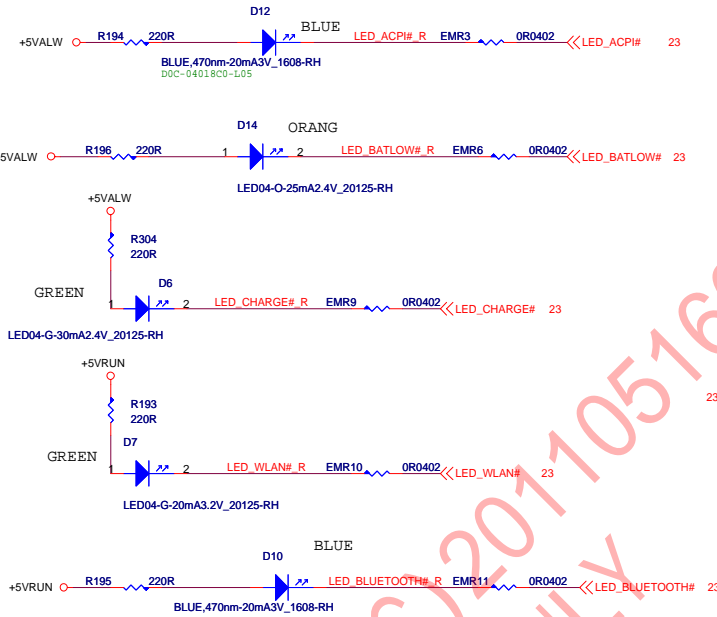
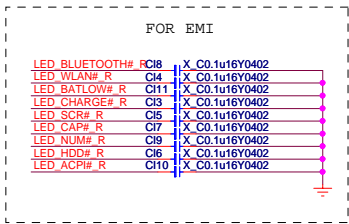
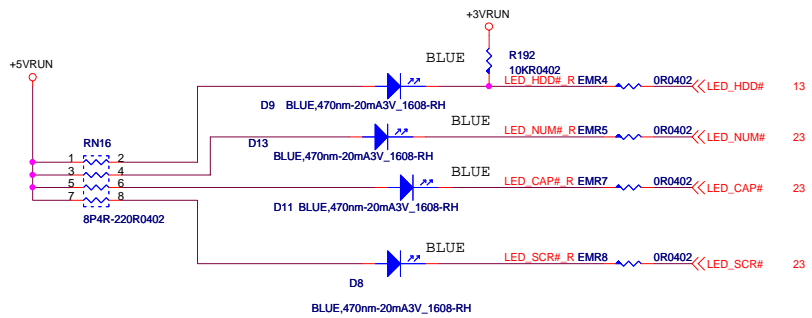
1. Pin 46 : RSET res should be close to LAN chip. Don't have power trace or high frequency trace beside it.
2. The trace of each Pair(MDIX+/-) should be equal in length and better have ground under.
3. Both EGND and GND can be connect together or use 0 Ohm res. to connect them.
4. 1.2V請留 power plane並且盡量大一點.
5. 1.2V Bypass 電容不能省. 在 LAN 的每一個 power pin 都加 0.1u 的電容, 不能省.
- 6.請參考RTL8111C EMI layout notice. Fine tune cap (0.1uF ~ 10pF) of center-tapped can improve EMI for single tone noise.
7. Please refer and follow our Layout Guidel.5 as attached file
8. RJ45 的部份,對應pin 請您在confirm一下.....一般都是接到 RJ45 pin 12/ 36



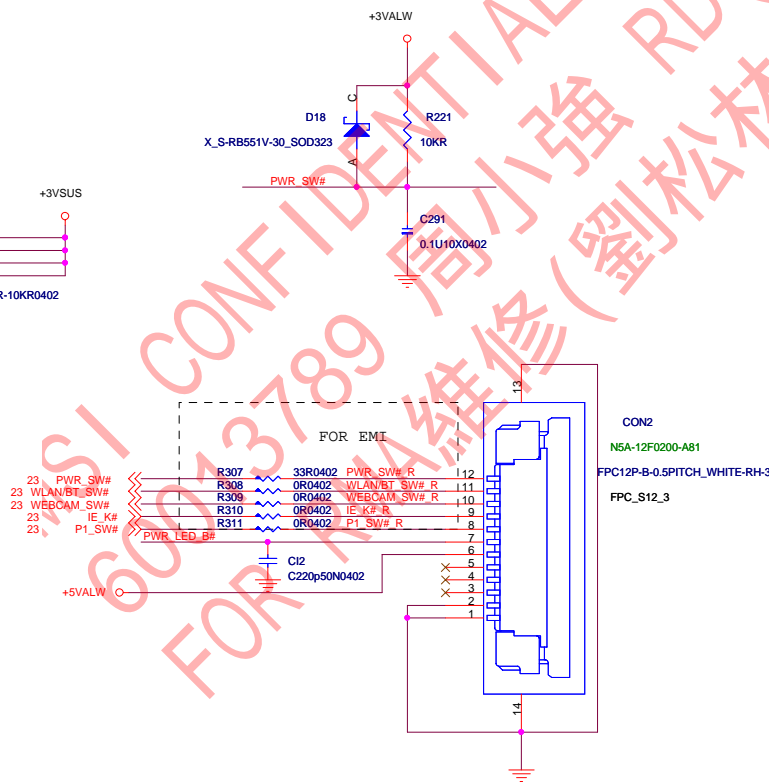
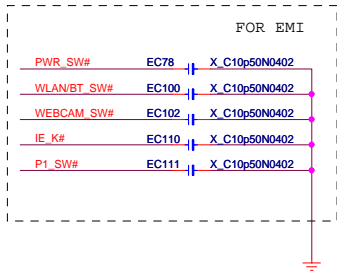
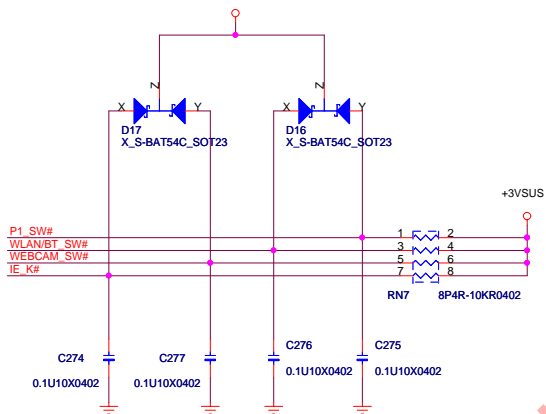
POWER Comparison

	3.3V	mW
10 M Idle/TxRx	87/172	287/568
100 M Idle/TxRx	112/165	370/545
ALDPS	60	198
D3 cold with link10M /without link	32/18	106/59.4

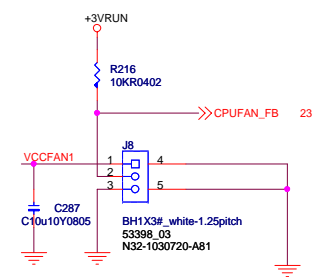
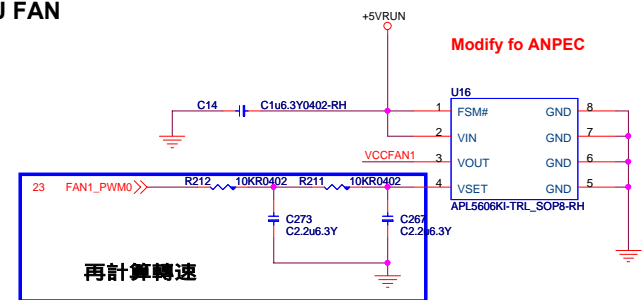




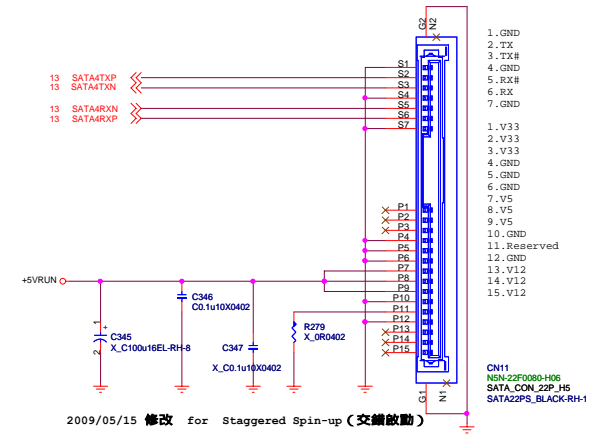
CLOSE TO CONNECTOR



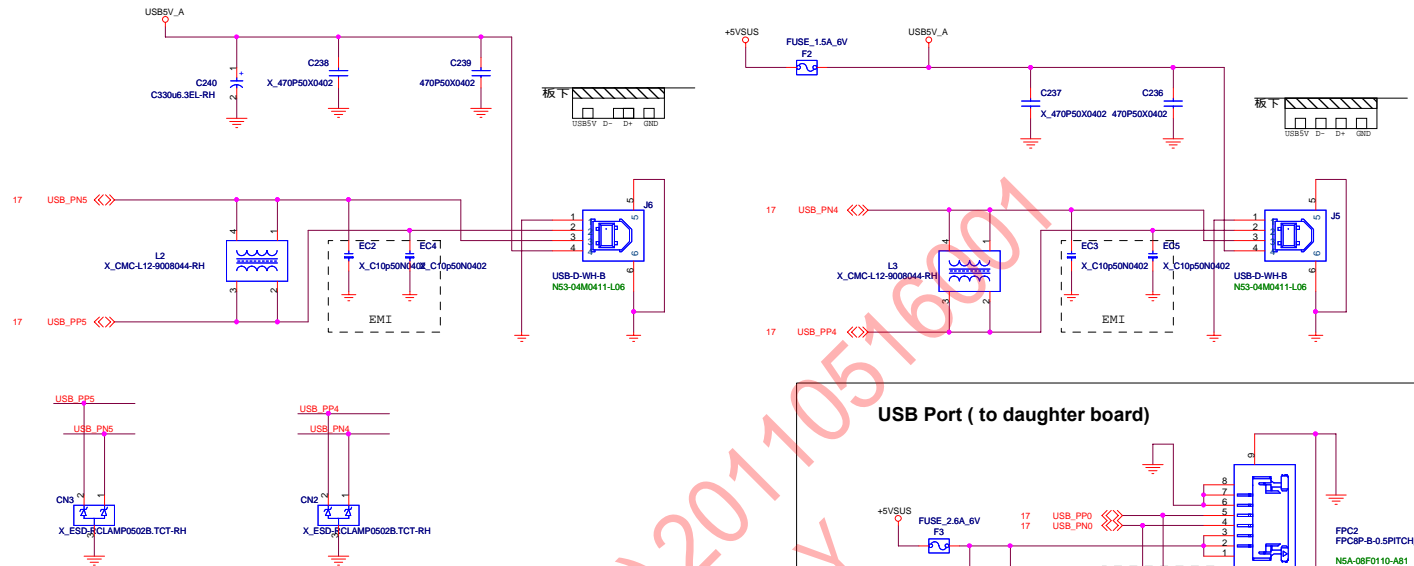
CPU FAN



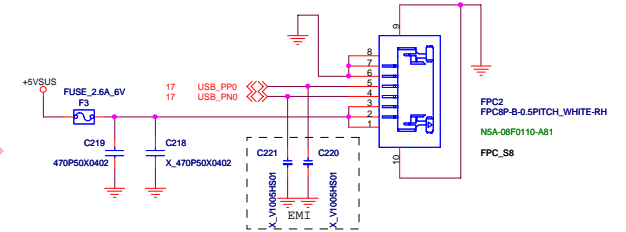
SATA HDD



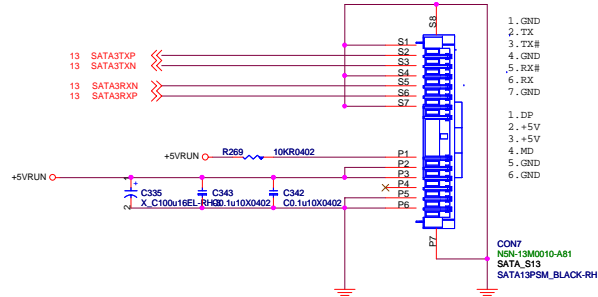
USB Port



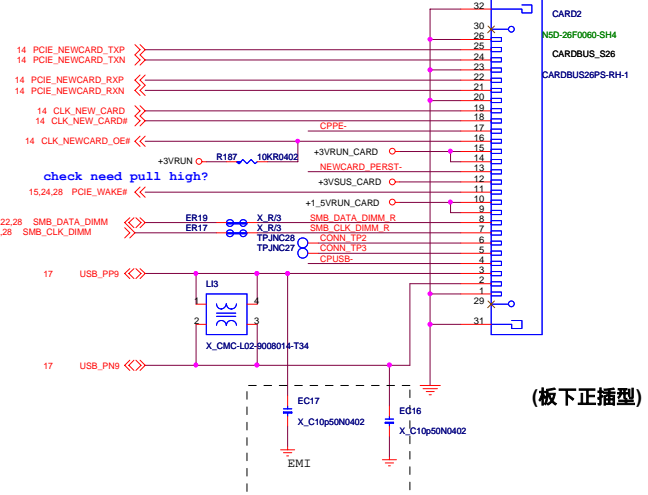
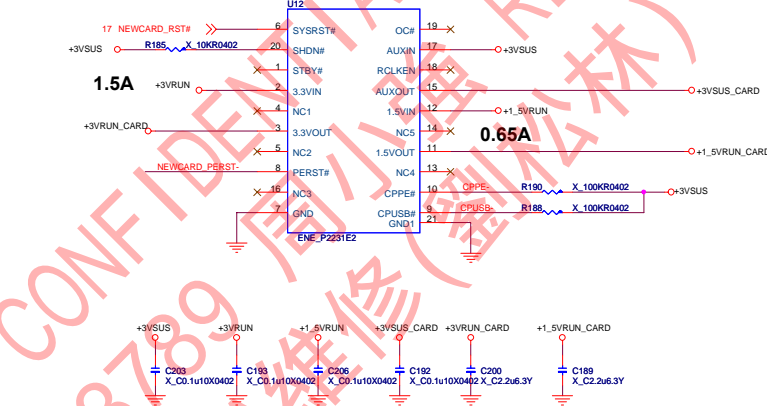
USB Port (to daughter board)



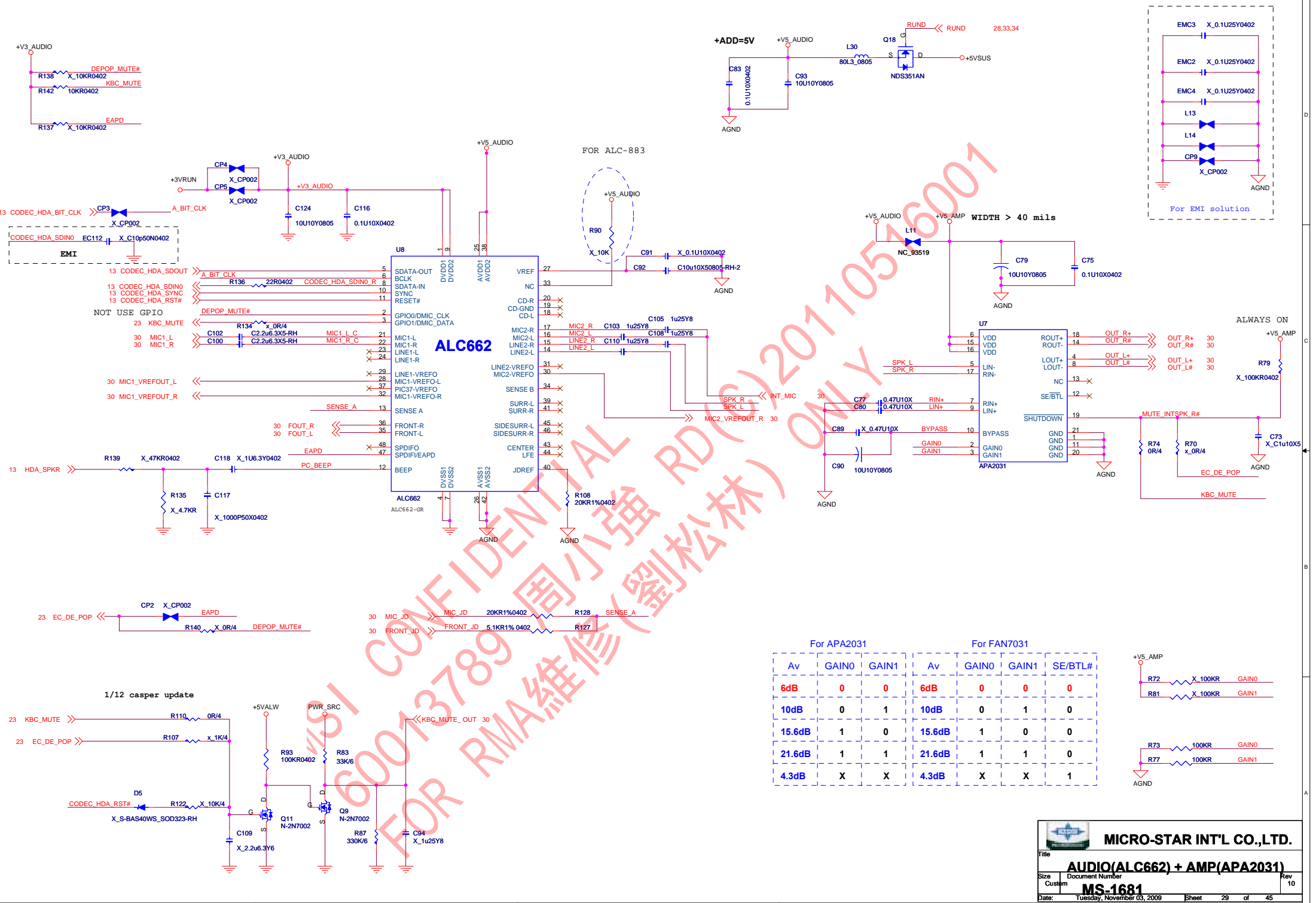
SATA ODD



NEW CARD



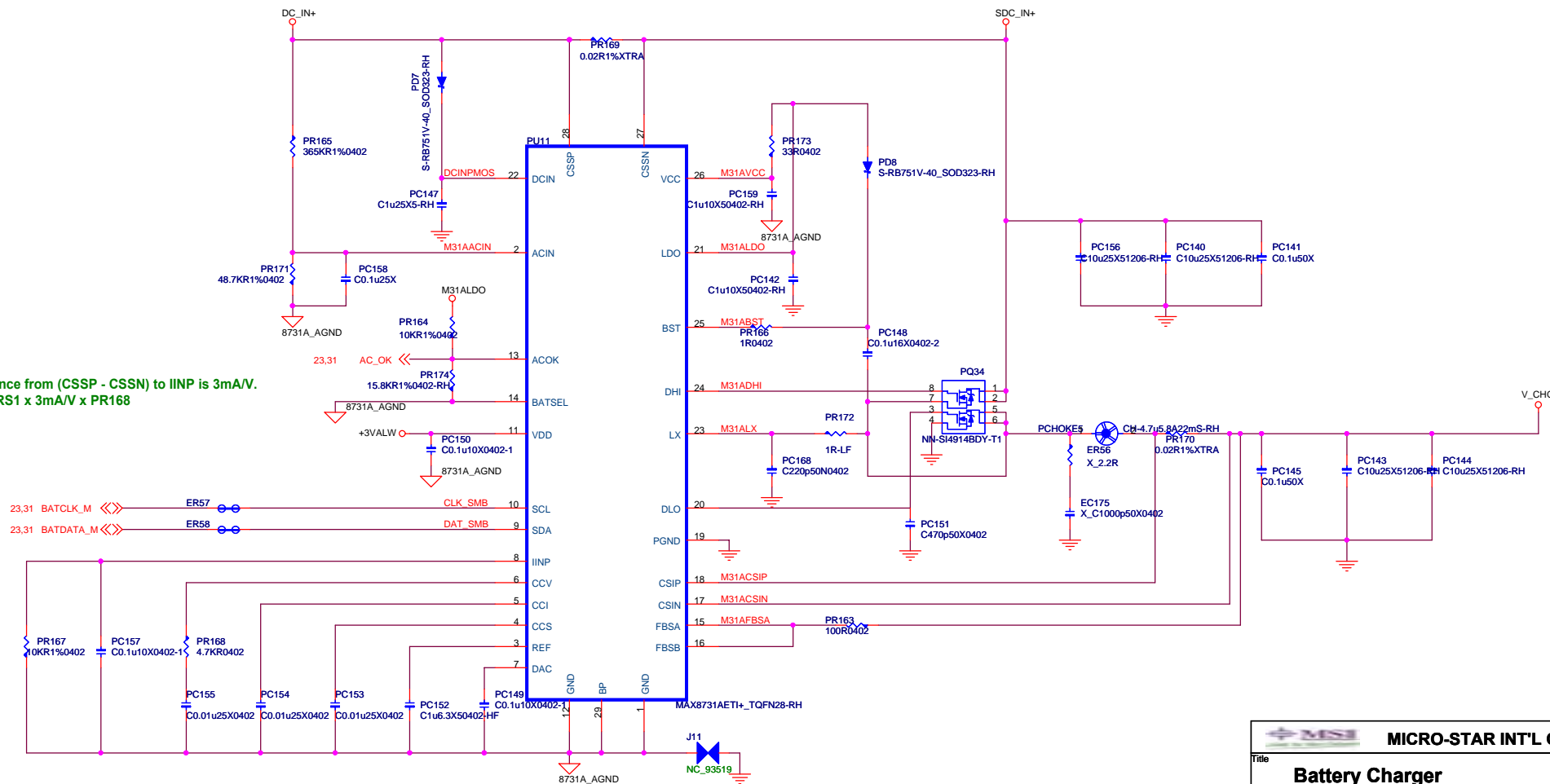
(板下正插型)




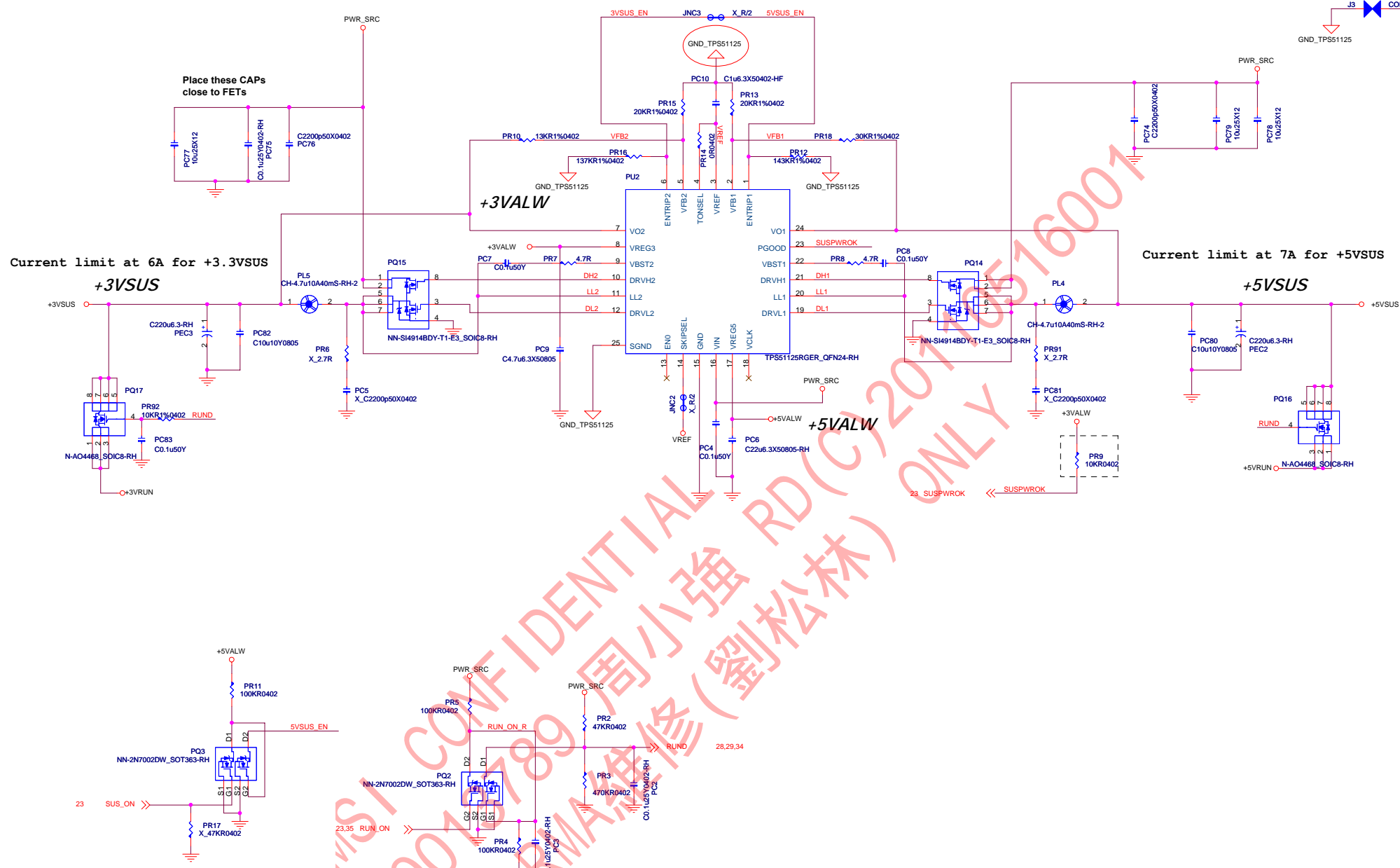
For APA2031				For FAN7031			
Av	GAIN0	GAIN1		Av	GAIN0	GAIN1	SE/BTL#
6dB	0	0		6dB	0	0	0
10dB	0	1		10dB	0	1	0
15.6dB	1	0		15.6dB	1	0	0
21.6dB	1	1		21.6dB	1	1	0
4.3dB	X	X		4.3dB	X	X	1

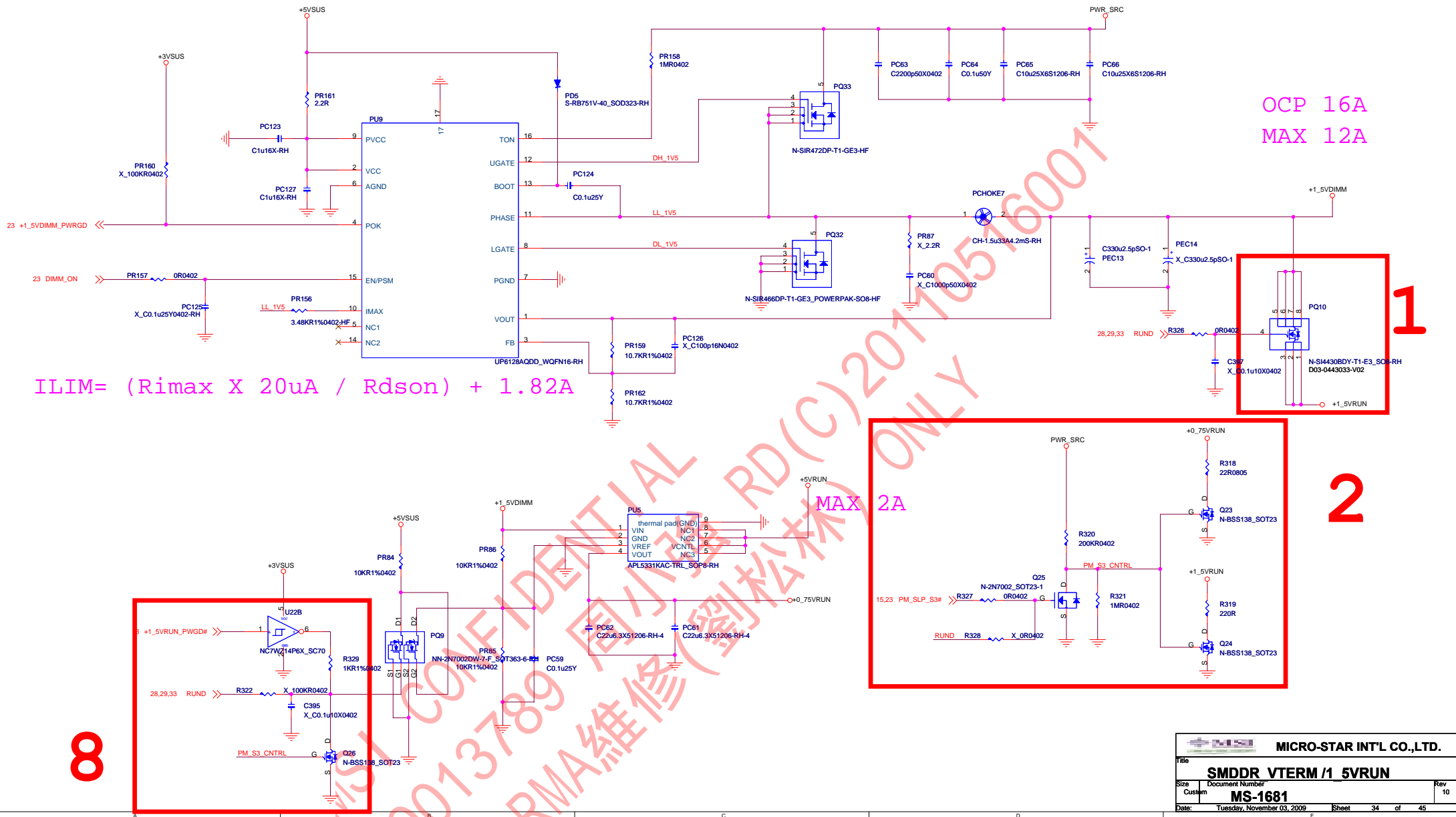
Adapter= 65W
Adapter input voltage set 19 Voltage

IINP :
1. The transconductance from (CSSP - CSSN) to IINP is 3mA/V.
2. $V_{IINP} = IINPUT \times RS1 \times 3mA/V \times PR168$



		MICRO-STAR INT'L CO.,LTD.	
Title			
Battery Charger			
Size	Document Number		Rev
Custom	MS-1681		10
Date:	Tuesday, November 03, 2009	Sheet	32 of 45

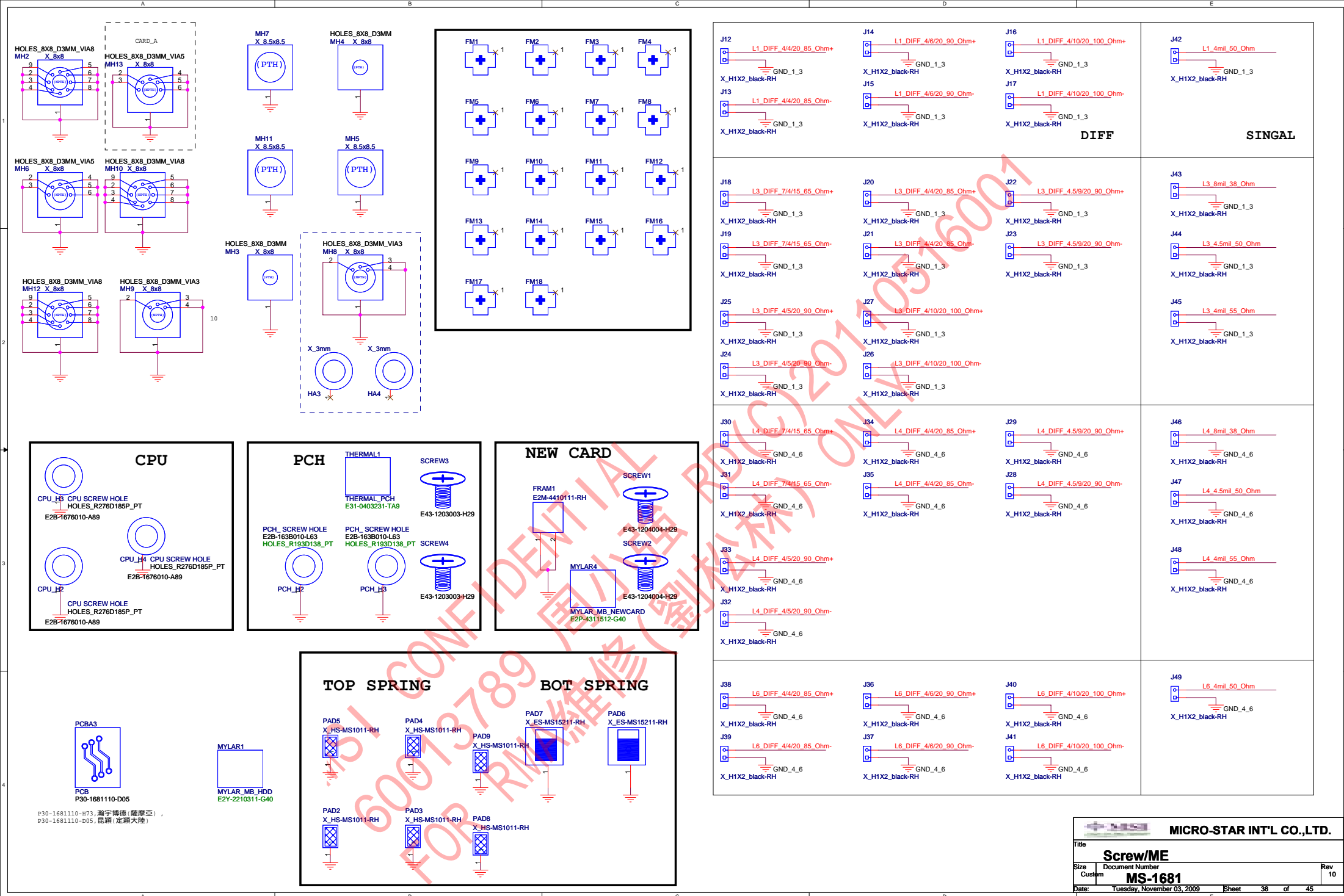


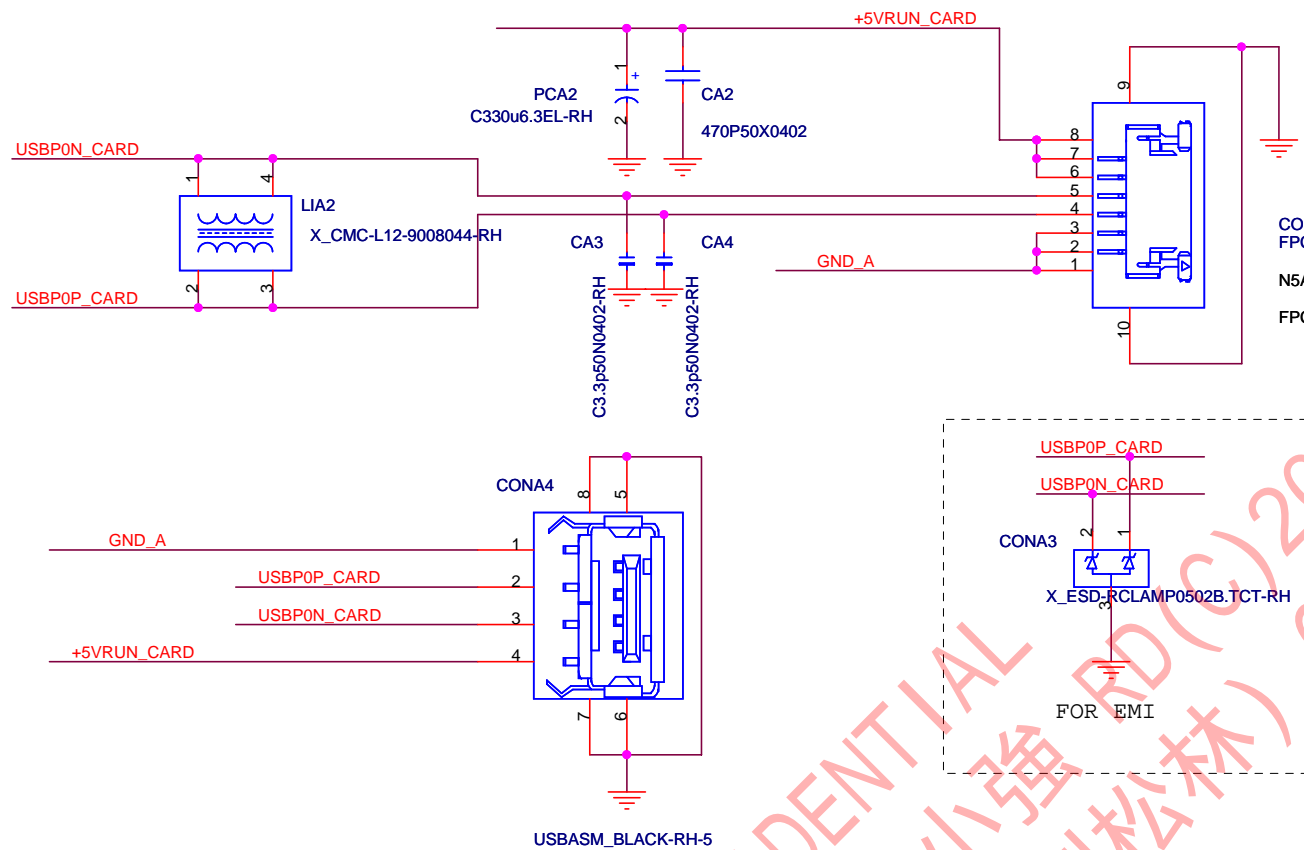


OCF 16A
MAX 12A

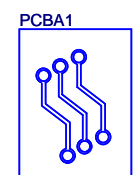
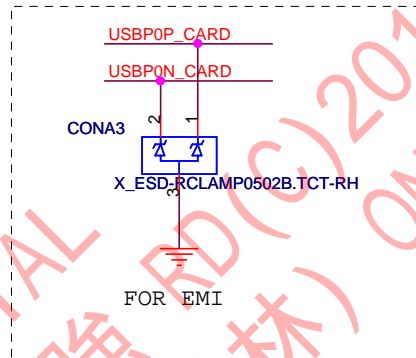
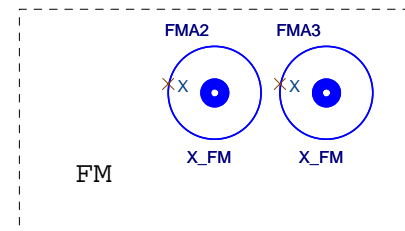
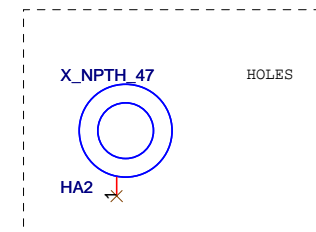
MAX 2A

MICRO-STAR INT'L CO.,LTD.			
Title			
SMDRR VTERM /1 5VRUN			
Size			
Document Number			
Custom			
MS-1681			
Date: Tuesday, November 03, 2009			
Sheet 34 of 45			
Rev 10			






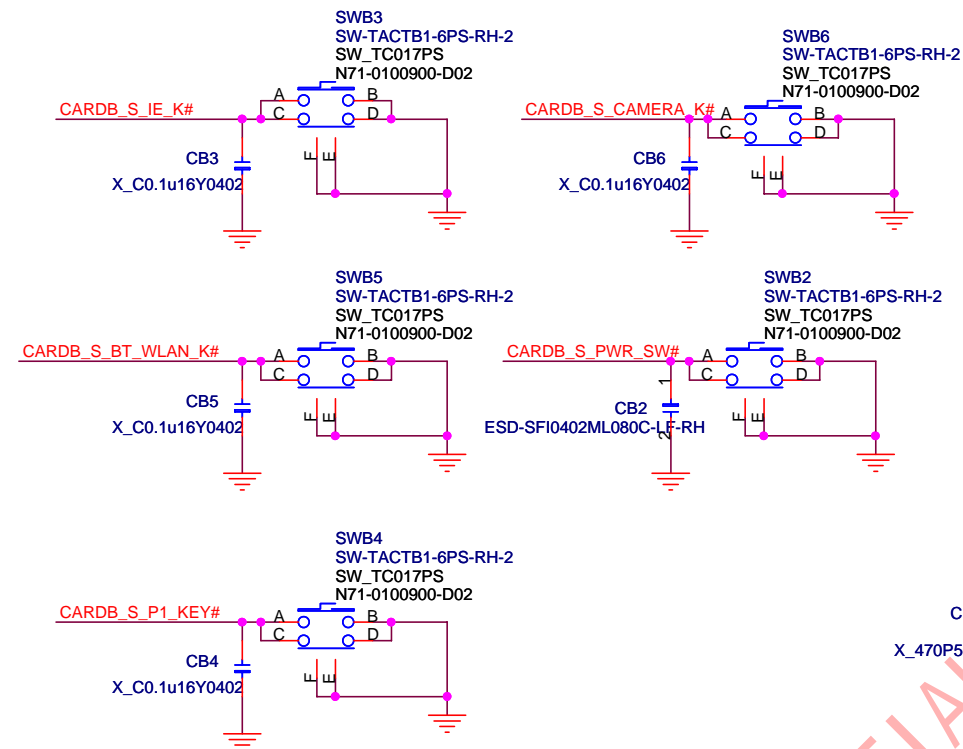
CARD_A USB0



PCB
P30-1681A10-D05

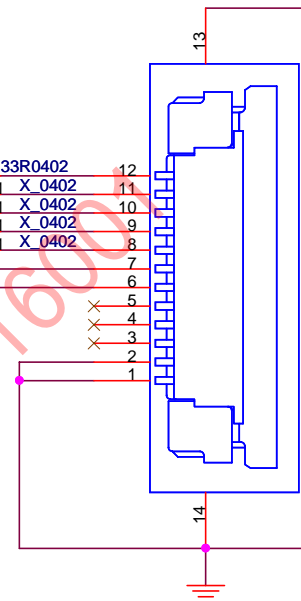
P30-1681A10-H73, 瀚宇博德 (薩摩亞)
P30-1681A10-D05, 昆穎 (定穎大陸)

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Title			
USB BOARD _A			
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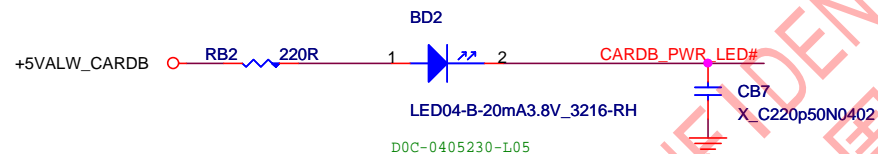


CARD_B_ BOTTOM

CARDB_S_PWR_SW#	RB3	33R0402	12
CARDB_S_BT_WLAN_K#	JNCB5	2	1 X 0402
CARDB_S_CAMERA_K#	JNCB6	2	1 X 0402
CARDB_S_IE_K#	JNCB3	2	1 X 0402
CARDB_S_P1_KEY#	JNCB4	2	1 X 0402
CARDB_PWR_LED#			7
+5VALW_CARDB			6
			5
			4
			3
			2
			1

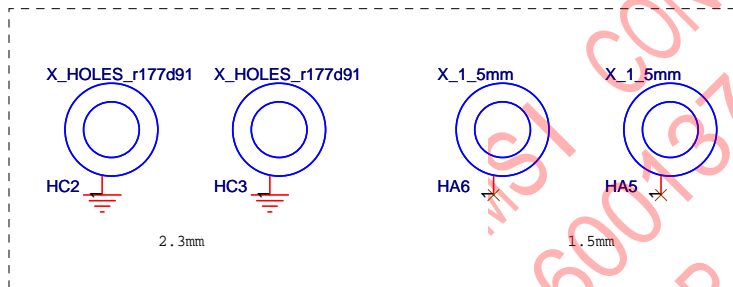


FPC3
FPC12P-B-0.5PITCH_WHITE-RH-3
N5A-12F0200-A81
FPC_S12_3




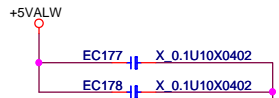
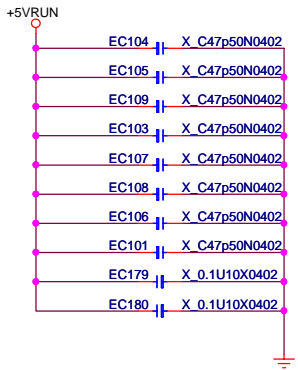
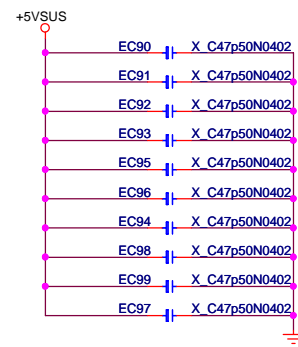
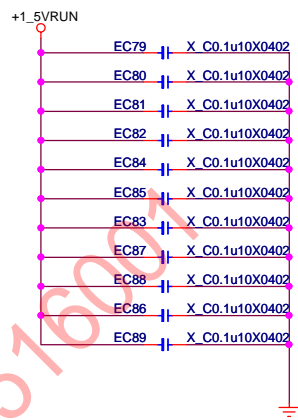
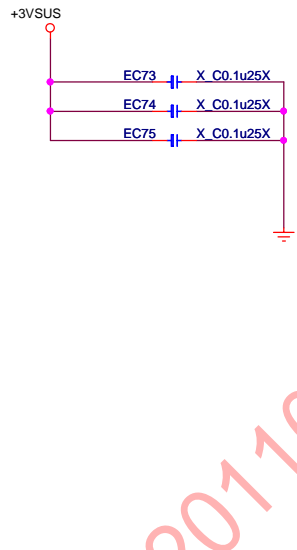
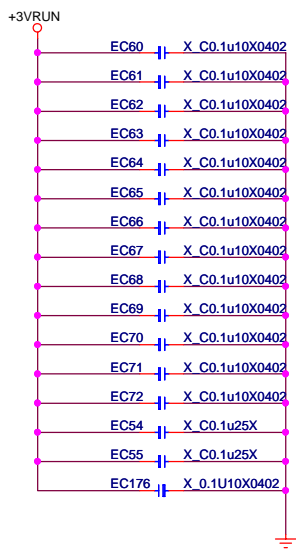
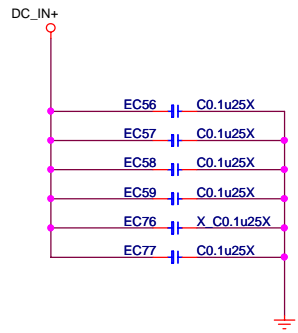
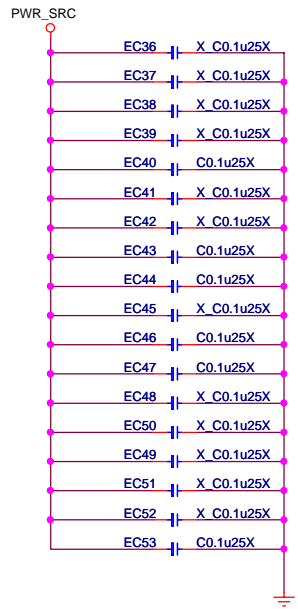
MYLAR2
MYLAR_BOTTOM_TOP
E2M-6811111-G40

MYLAR3
MYLAR_BACK
E2P-6811311-G40



P30-1681B10-H73, 瀚宇博德 (薩摩亞)
P30-1681B10-D05, 昆穎 (定穎大陸)

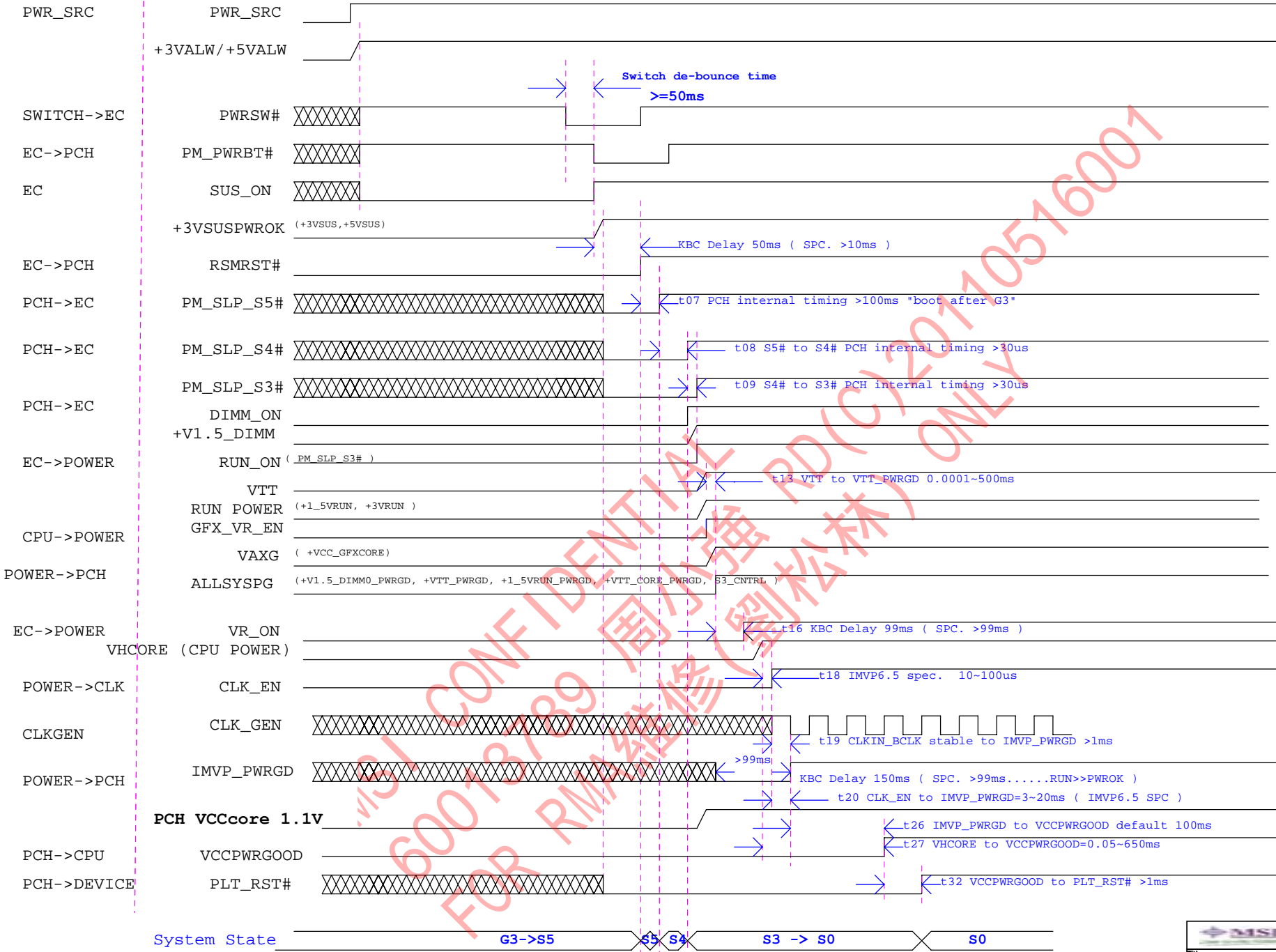
		MICRO-STAR INT'L CO.,LTD.		
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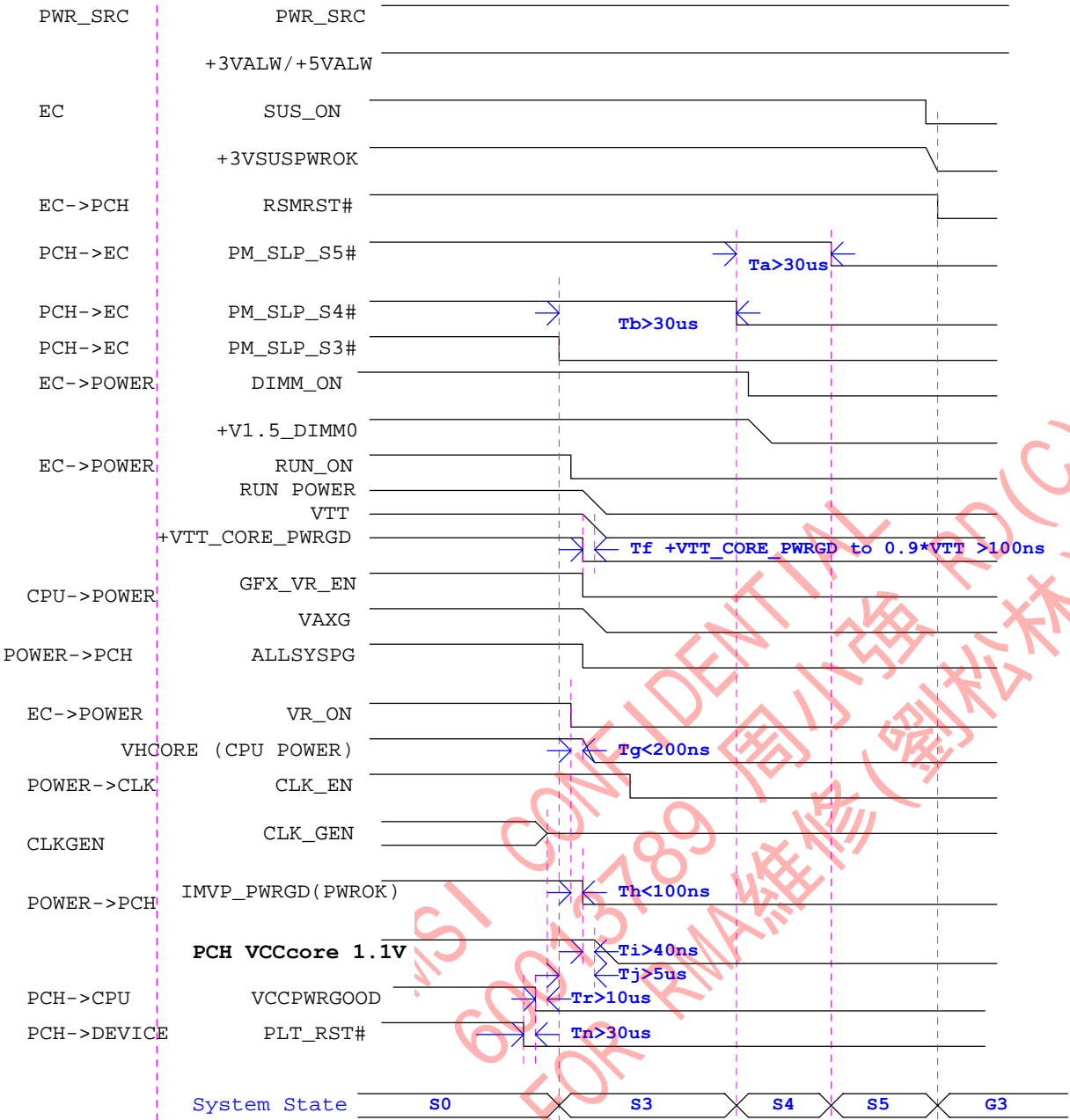
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60013789 周小強 (劉松林) ONLY
FOR RMA維修

MSI MICRO-STAR INT'L CO.,LTD.		Title EMI	
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Calpella System Power on Sequence DC mode



Power down Sequence DC mode S0 to G3




Change Note :

0A-->0B

- 1.P19 stuff R113 & C85 for intel document about Braidwood
- 2.P23 add one PWM Pin for co-lay LED panel by EC
- 3.P25 Change CardReader to ENE
- 4.P26 Change "LED_HDD#" PU +5VRUN to +3VRUN
- 5.P26 Fan conn footprint change back to "53398_03"
- 6.P28 Add Wireless & Bluetooth combo(MS-3870)
- 7.P32 Change PR171 to 48.7K & PR172 to 1R0603
- 8.P33 Change PU2 from "UP6182AQAG" to "TPS51125" & PR18 to 30K
- 9.P34 Change PU9 from "UP6111AQDD" to "UP6128A" & PR156 to 3.48K & PR159 to 10.7K & PQ10 to "D03-0443033-V02"
- 10.P35 Change PU8 from "UP6111AQDD" to "UP6128A" & PR149 to 4.22K & remove C394
- 11.P36 Change PR95 to 1.82K & PR29 to 9.31K & PC90 to 47nf & PR99 to 931R & no stuff PC84 , PR94 , PEC4 , PEC5 , PEC6 , PEC8

0B-->10

- 1.P13 add net "TP_HDA_DOCK_EN#_R" for flash protect control.
- 2.P14 add wimax ac adepter schematic.
- 3.P23 add ENE GPIO13 for flash protect control.
- 4.P25 no stuff C399 & C400 for cardreader detect issus.
- 5.P26 change R307 from 0R to 33R for EMI.
- 6.P31 add 2 cap in +VBATA for EMI.
- 7.P34 change R329 from 0R to 1K for current limit.
- 8.P37 no stuff +VCC_GFXCOPE PQ23 no cost down.
- 9.P40 change JNCB2 to RB3 , and 33R for EMI.
- 10.P40 change CB2 from 0.1u to 300p for EMI.

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